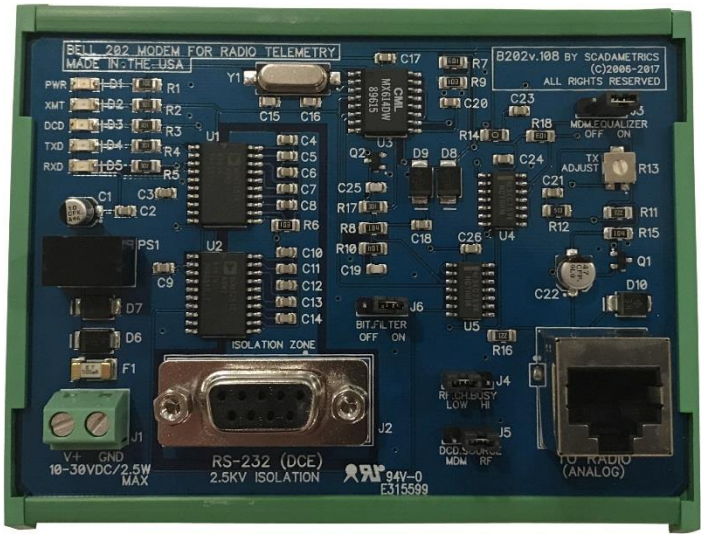
SCADAMETRICS

Bell 202 Modem

DIGITAL COMMUNICATIONS FOR RADIO TELEMETRY



MADE IN USA

2 YEAR WARRANTY

Standards-Based, Non-Proprietary Modem For Radio Telemetry...

The SCADAmetrics Model B202 Modem is designed to provide non-proprietary, Bell-202 data modulation and demodulation for many popular analog telemetry radios.

The unit offers the following notable features:

- Wide-Input Power Range 10-30VDC.
- 2.5KV Isolated Serial Port for RS-232 Interface to PLC/RTU/Computer.
- Serial Port Pins 4-6, 7-8 Jumpered for Rockwell/Allen Bradley Compatibility.
- Radio Interface: RJ45F.
- Industrial Din-Rail Mount.
- LED's: Power, Transmit, Receive, TxD, RxD.
- Adjustable Transmit Audio Level: 0-2V Peak-to-Peak Signal. Able to Drive 600-∞ Ω Loads.
- Selectable RF or Modem Carrier Detect.
- Carrier-Detect Byte Filtering Option.
- Receive Signal Equalizer Option.
- 'Dumb' Mode Operation.

The B202 modem permits users to mix various makes and models of compatible radios within a telemetry system, thereby alleviating the problem of vendor lock-in.

This new design is based upon the MX614 modem IC (CML Micro), and it is also fully compatible with legacy Bell-202 modems that are based upon the TCM3105 modem IC (Texas Instruments), such as the Calamp DM-3282, Maxon SD-FSK, and MARC 366-101. Compatibility is anticipated with a wide range of popular analog telemetry radios, including models from the following manufacturers:

- Ritron
- Tecnet / Maxon
- GE / Microwave Data Systems
- Calamp
- RF Neulink

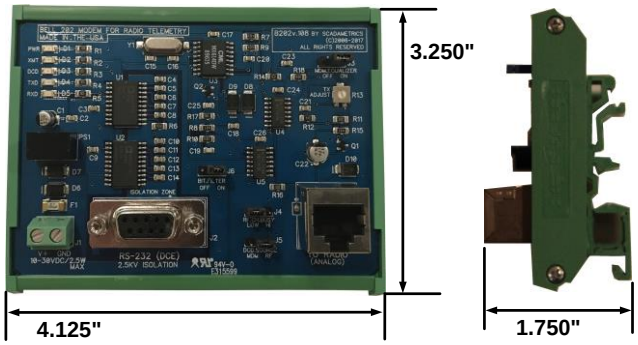
In accordance with FCC CFR 47 Part 15.103(a,b,c) – the B202 is only intended to be used as a control system component at public utility facilities, industrial plants, and within commercial transportation vehicles. It is also intended to be used within industrial, commercial, & medical test equipment. Not intended for consumer applications.

SCADAmetrics
scadametrics.com
St. Louis, Missouri USA
(636)405-7101

Specifications…

Mechanical/Electrical

Manufacturing Location:	USA
Dimensions:	4.125" x 3.250" x 1.750"
Weight:	3.8 Ounces
Temperature:	-30C to +85C
Relative Humidity:	5% to 95%, Non-Condensing
Panel Mounts:	Two (2) Universal Din-Rail Clips
Supply Voltage/Power:	10VDC to 30VDC, 1.50W max
Supply Current:	100mA @ 12VDC, Typical 50mA @ 24VDC, Typical
Serial Port Isolation:	2.5 KV
Term. Blk. Conductors:	16AWG Max, 26AWG Min
Internal Power Efficiency:	90%, Typical
Circuit Protection:	Fused (375mA) + TVSS Diode + Reverse-Polarity Protection Diode
Audio Output Signal Level:	0-2V peak-to-peak (0-.708Vrms), Adjustable. 600-∞ Ohm Loads.



Serial Communications

Interface Port:	**RS-232C (DB9F Jack, DCE):** 1: **DCD** (Transmitted to DTE) 2: **TxD** (Transmitted to DTE) 3: **RxD** (Received from DTE) 4: DSR (TIED TO DTR) 5: **GND** 6: DTR (TIED TO DSR) 7: **CTS** (TIED TO RTS) 8: RTS (TIED TO CTS) 9: N/C
Speed:	300 to 1200 bps
Handshaking:	None (Requires External RTS/PTT Control)
Protocol Compatibility:	MODBUS, DF1, Custom Binary & ASCII Protocols

Radio Communications

Modulation Type:	AFSK (Audio Frequency Shift Key), Bell-202
Interface Port:	**RJ-45F:** 1: TxAudio (Adj: 0-2 Vpp / 0-0.708 Vrms) 2: RxAudio 3: PTT (Active Low) 4: Channel Busy 5: Ground 6: N/C 7: N/C 8: DC Power (Non-Fused, Mapped from V+ Terminal)

Configuration Jumpers

RF.CH.BUSY Normal (~5V=BUSY)	JP1 = HI
RF.CH.BUSY Inverted (0V=BUSY)	JP1 = LOW
(Sets Polarity of Radio Channel Busy/Carrier Detect)	
DCD.SOURCE = RF Channel Busy	JP2 = RF
DCD.SOURCE = Modem Energy Detect	JP2 = MDM
(Sets The Source Of DCD Signal: Radio or Modem)	
BIT.FILTER ON	JP3 = ON
BIT.FILTER OFF	JP3 = OFF
(BIT.FILTER ON: Data Only Passed Thru When DCD Asserted)	
MDM.EQUALIZER ON	JP4 = ON
MDM.EQUALIZER OFF	JP4 = OFF
(Modem Equalizer – See Explanation On Page 6 of MX614 Datasheet)	

FAQ's…

- **Is the B202 a 'smart' modem?** No, the B202 modem is a 'dumb' modem. The benefits are total control of the modulation and demodulation process and enhanced ability to troubleshoot. However, a 'dumb' modem requires the user to key the transmitter through software prior to and during data transmission using the RTS serial port pin. The user also must provide logic to detect and separate valid packets from extraneous noise. This is typically done by framing each packet with a pre-determined byte sequence.

- **What are the power requirements of the B202?** The B202 provides the user with a great deal of flexibility in that it will operate on any voltage between 10-30VDC. However, it is almost always preferable that the user power the modem with the same voltage source that is used to power the radio – which will generally be ~12VDC. Pin 8 of the RJ45 jack provides a direct connection back to the V+ terminal block. If the radio is to be powered with a separate voltage source, then it is imperative that Pin 8 of the RJ45 jack should not be connected to the radio.

- **Does the B202 require programming?** No, the unit features 4 jumpers for tailoring the modem to your radio and application, and one trim pot for adjusting the transmit audio level.

- **Do you offer radio interface cables?** Yes. Because many of the popular telemetry radios feature DB9, DB25, or DB15 interface ports; and it's now extremely easy and popular to create custom cable assemblies with RJ45F-to-DSub Adapters. This allows us to offer cable assemblies for many popular telemetry radios. Our cable assemblies generally consist of an RJ45F-DSub Adapter and a premium shielded CAT5 patch cable (24-gauge, solid-copper conductors).

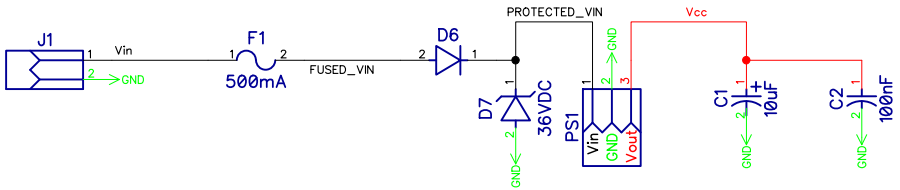
- **What documentation is available?** The B202 is offered as a non-proprietary modem device whose operation can be troubleshot and repaired by qualified technical personnel. For this reason, complete documentation is provided – including operations manual, schematics, and the modem IC datasheet.

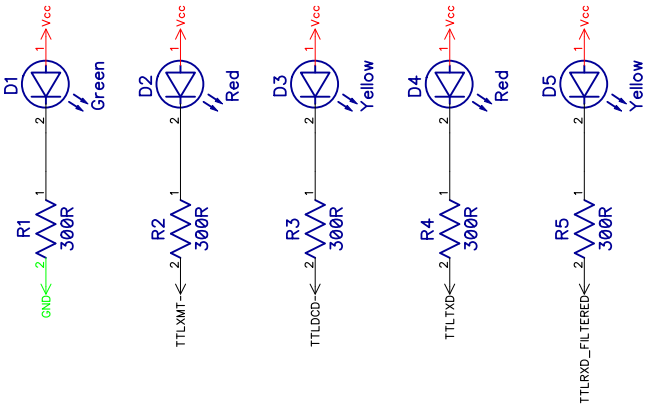
- **What are the Bell-202 modulation tones?** The Bell-202 standard uses 1200 Hz for 'MARK' (Binary '1'), and 2200 Hz for 'SPACE' (Binary '0').

SCADAmetrics
scadametrics.com
St. Louis, Missouri USA
(636)405-7101

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

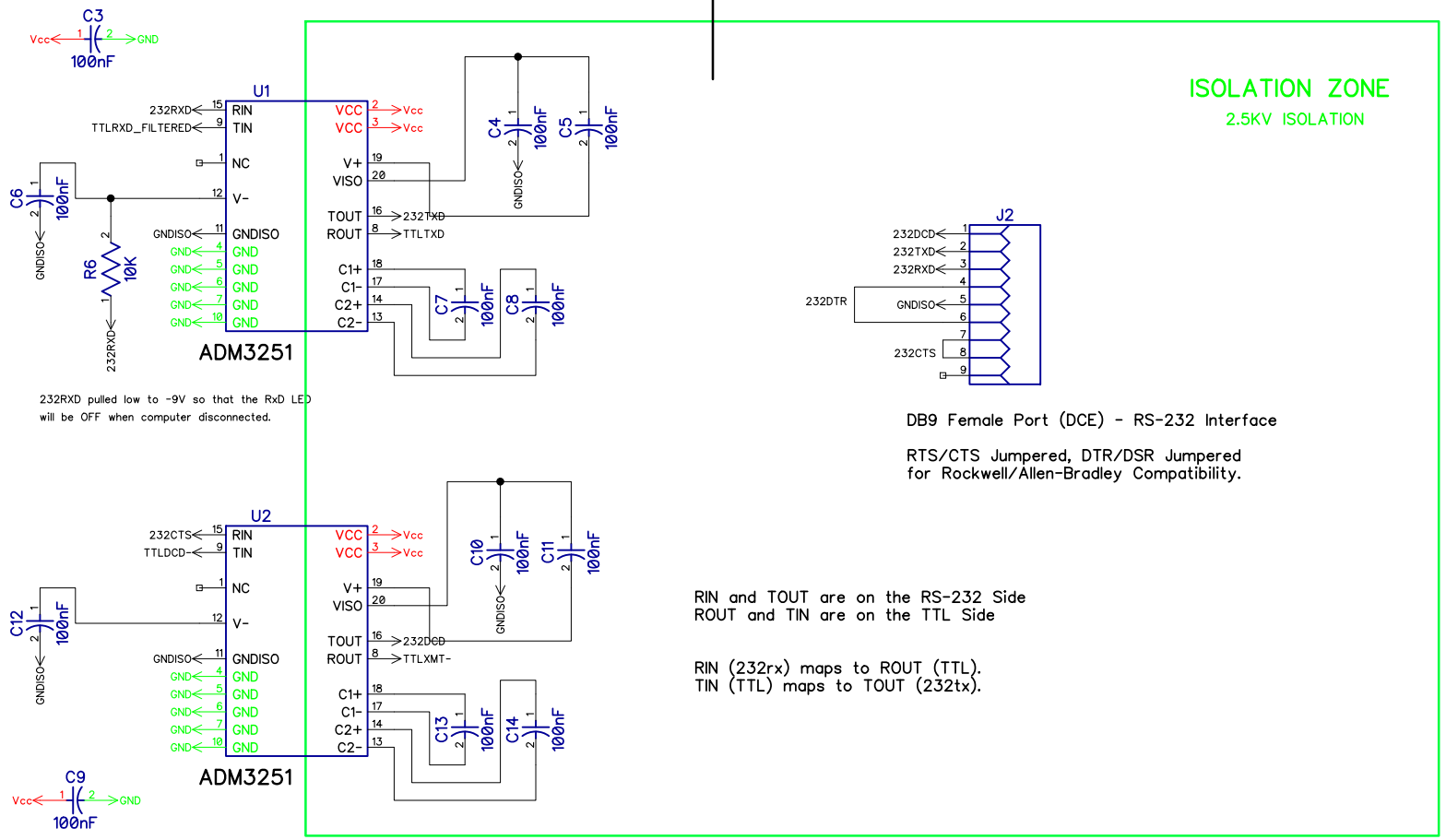
PHOENIX TERMINAL BLOCK
POWER (10-30VDC, 0.5W MAX)





Engineer: Jim Mimlitz SCADAmetrics		Model No. B202 Bell 202 Modem for Radio Telemetry		
27 June 2017	SIZE	FSCM NO.	DWG NO. 1 of 4	REV 108
	SCALE		Power	

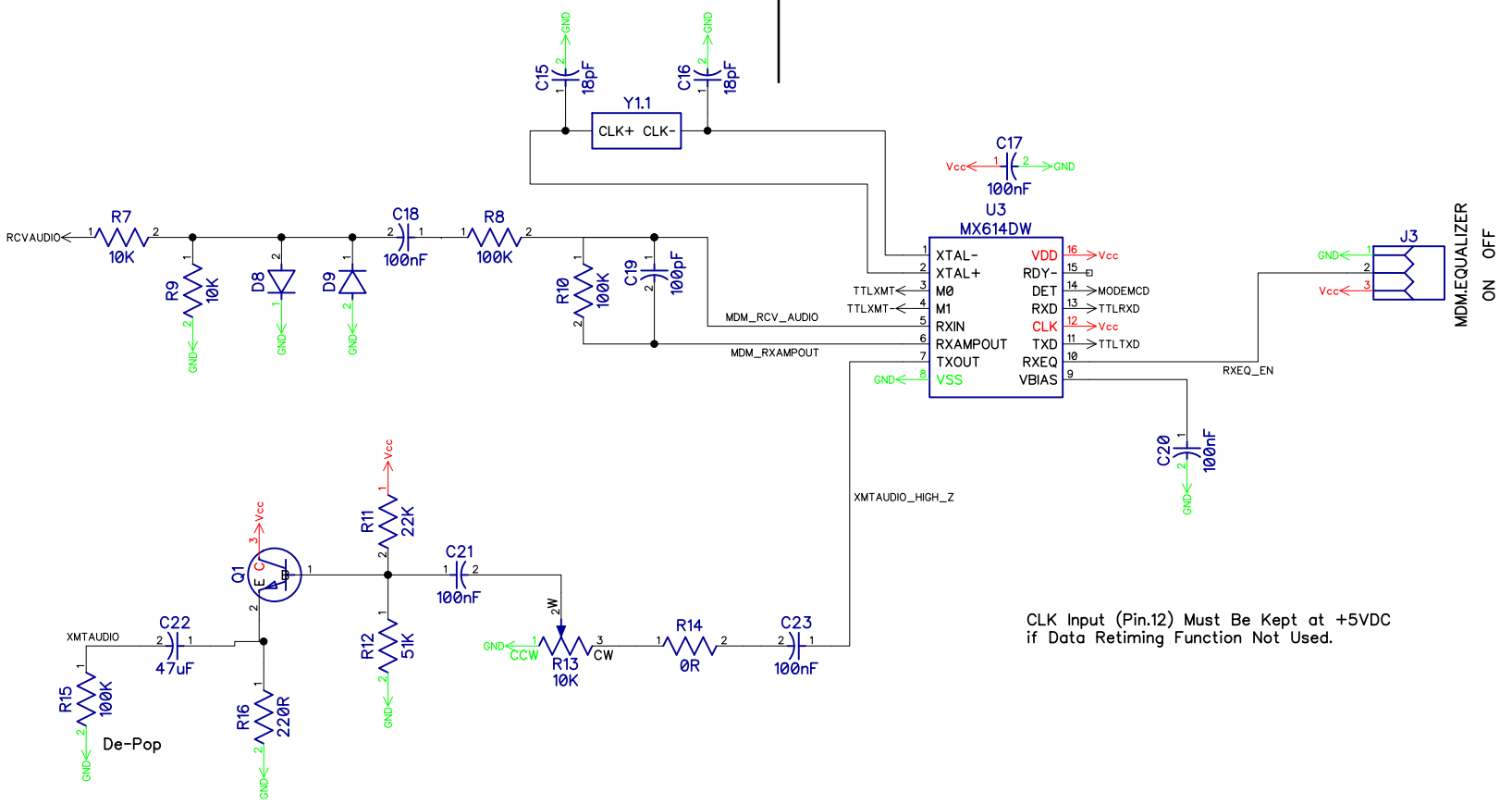
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED



TTLRXD_FILTERED enters the ADM3251,
and is translated to 232TXD.

232RXD enters the ADM3251,
and is translated to TTLTXD (Radio Transmitter).

Engineer: Jim Mimlitz SCADAmetrics	
	Model No. B202 Bell 202 Modem for Radio Telemetry
27 June 2017	SIZE: — FSCM NO. — DWG NO. 2 of 4 — REV 108
	SCALE — RS-232



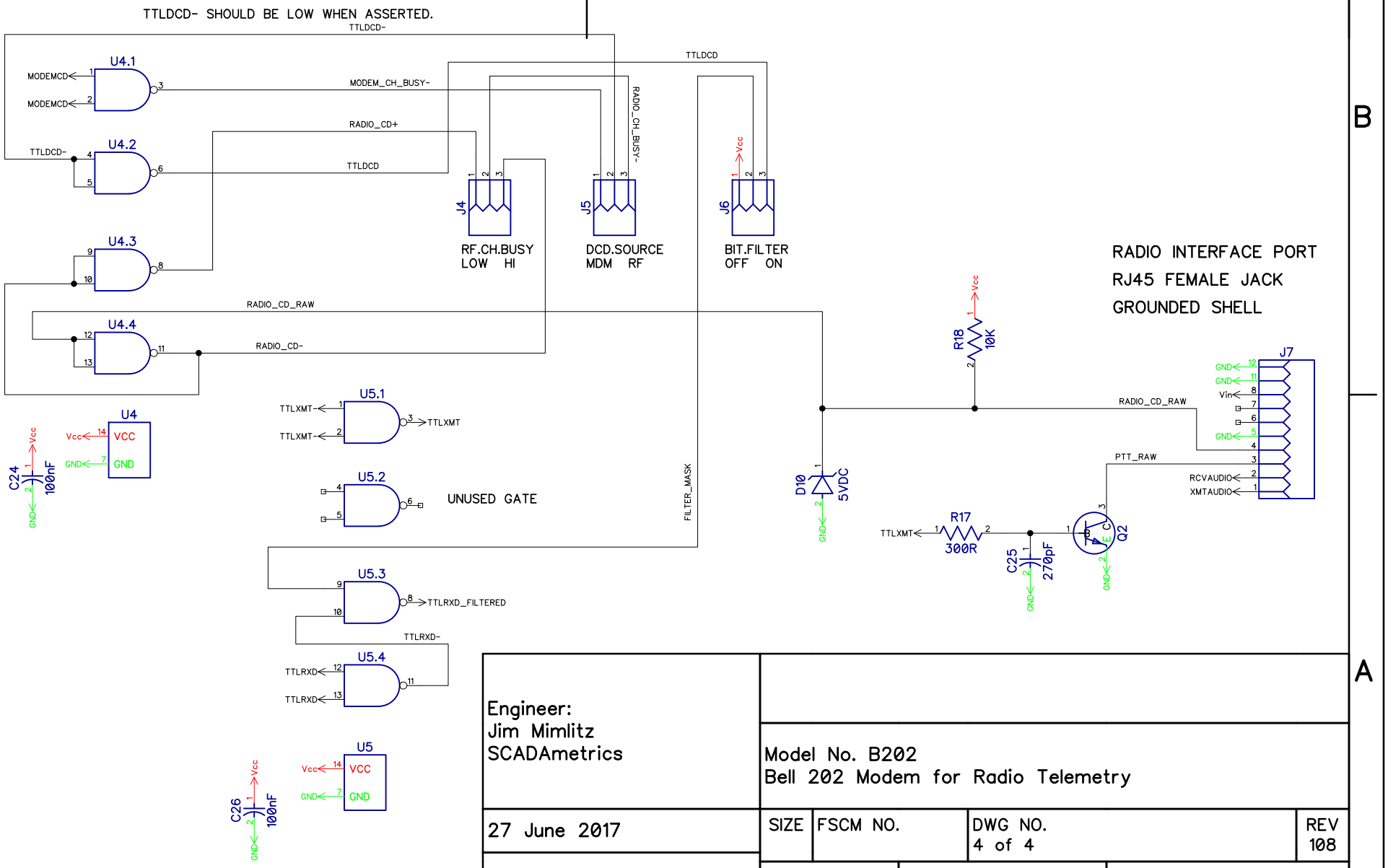
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

Engineer:
Jim Mimlitz
SCADAmetrics

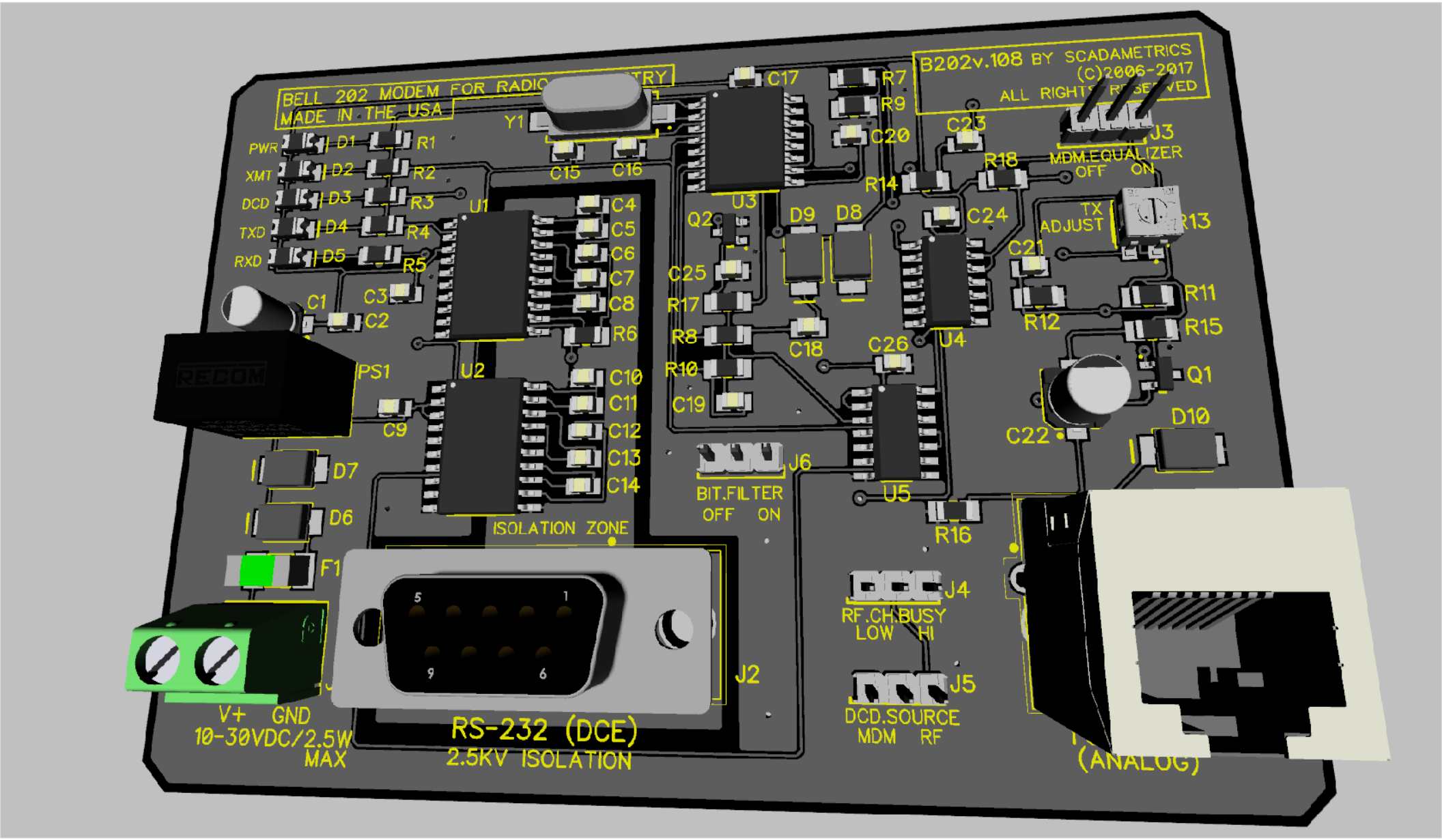
27 June 2017

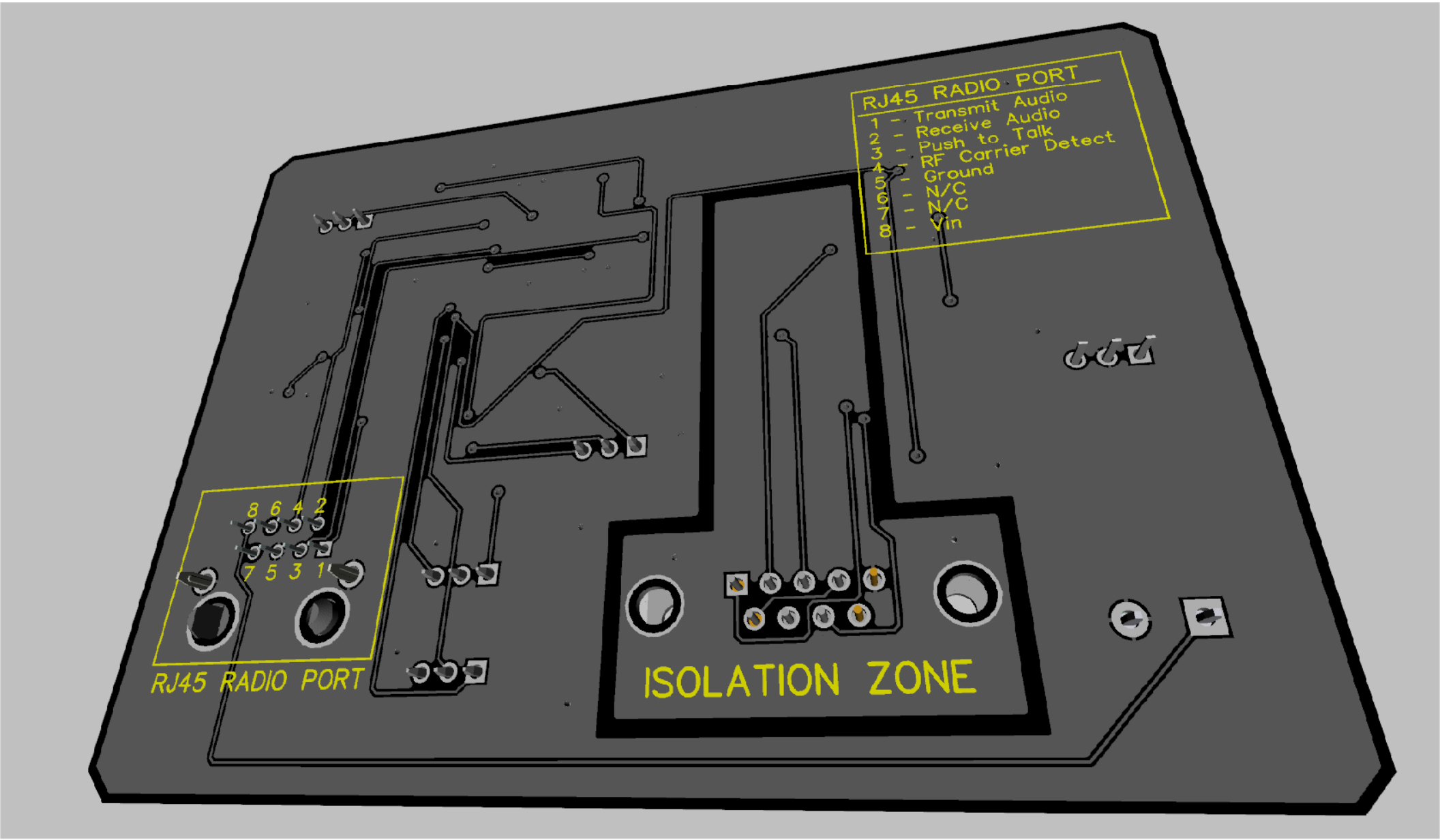
Model No. B202
Bell 202 Modem for Radio Telemetry

SIZE	FSCM NO.	DWG NO.	REV
		3 of 4	108
SCALE		Modem	



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED


BELL 202 MODEM FOR RADIO
MADE IN THE USA
B202v.108 BY SCADAMETRICS
(C)2006-2017
ALL RIGHTS RESERVED
PWR
XMT
DCD
TXD
RXD
D1
D2
D3
D4
D5
R1
R2
R3
R4
R5
Y1
C15
C16
C17
U1
U2
U3
U4
U5
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
R6
R7
R8
R9
R10
C18
C19
C20
C21
C22
C23
C24
C25
C26
R11
R12
R13
R14
R15
R16
R17
R18
Q1
Q2
D6
D7
D8
D9
D10
F1
PS1
RECOM
J2
J3
J4
J5
J6
MDM.EQUALIZER
OFF ON
TX
ADJUST
BIT.FILTER
OFF ON
ISOLATION ZONE
RF.CH.BUSY
LOW HI
DCD.SOURCE
MDM RF
V+ GND
10-30VDC/2.5W
MAX
RS-232 (DCE)
2.5KV ISOLATION
(ANALOG)


RJ45 RADIO PORT
1 - Transmit Audio
2 - Receive Audio
3 - Push to Talk
4 - RF Carrier Detect
5 - Ground
6 - N/C
7 - N/C
8 - Vin
8 6 4 2
7 5 3 1
RJ45 RADIO PORT
ISOLATION ZONE

MX•COM, INC.
COMMUNICATION SEMICONDUCTORS

MX614

DATA BULLETIN

Bell 202 Compatible Modem

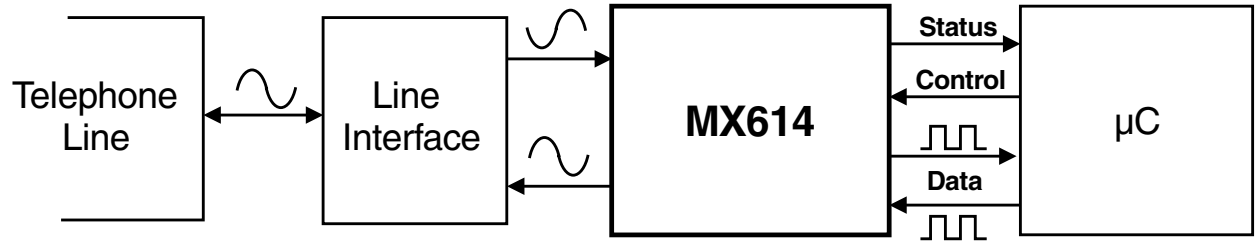
PRELIMINARY INFORMATION

Features

- **1200bps - 1800bps half duplex Bell 202 Compatible Modem**
- **Optional 1200bps Data Retiming Facility can eliminate external UART**
- **Optional 5bps and 150bps Back Channel**
- **Optional Line Equalization**

Applications

- **Low Voltage Operation (3.3V to 5.0V)**
- **Low Power Operation**
  - **1mA typ. @ 3.3V Operating Mode**
  - **1μA typ. Zero-Power Mode**
- **Standard 3.58MHz Xtal/Clock**
- **Telephone Telemetry Applications**



The MX614 is a low voltage, low power CMOS integrated circuit designed for the reception or transmission of asynchronous 1200bps data. This device is compatible with Bell 202 type systems. The MX614 supports 5bps and 150bps 'back channel' operation. Asynchronous data rates up to 1818bps are also supported.

The MX614 provides an optional Tx and Rx data retiming function which can eliminate, based on user preference, the need for a UART in the associated μC when operating at 1200bps. An optional line equalizer has been incorporated into the receive path and is controlled by an external logic level.

The MX614 may be used in a wide range of telephone telemetry systems. A very low current "Zero Power Mode (1μA typ.) and an operating current of 1mA typ. @ V_{DD} = 3.3V, make the MX614 ideal for portable, terminal and line powered applications. A standard 3.58MHz Xtal/Clock is required and the device operates from a 3.0V to 5.5V supply.

The MX614 is available in 24-pin TSSOP (MX614TN), 16-pin SOIC (MX614DW) and 16-pin PDIP (MX614P) packages.

www.mxcom.com Tel: 800 638 5577 336 744 5050 Fax: 336 744 5054
4800 Bethania Station Road, Winston-Salem, NC 27105 USA
Doc. # 20480162.004

CONTENTS

Section **Page**

MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

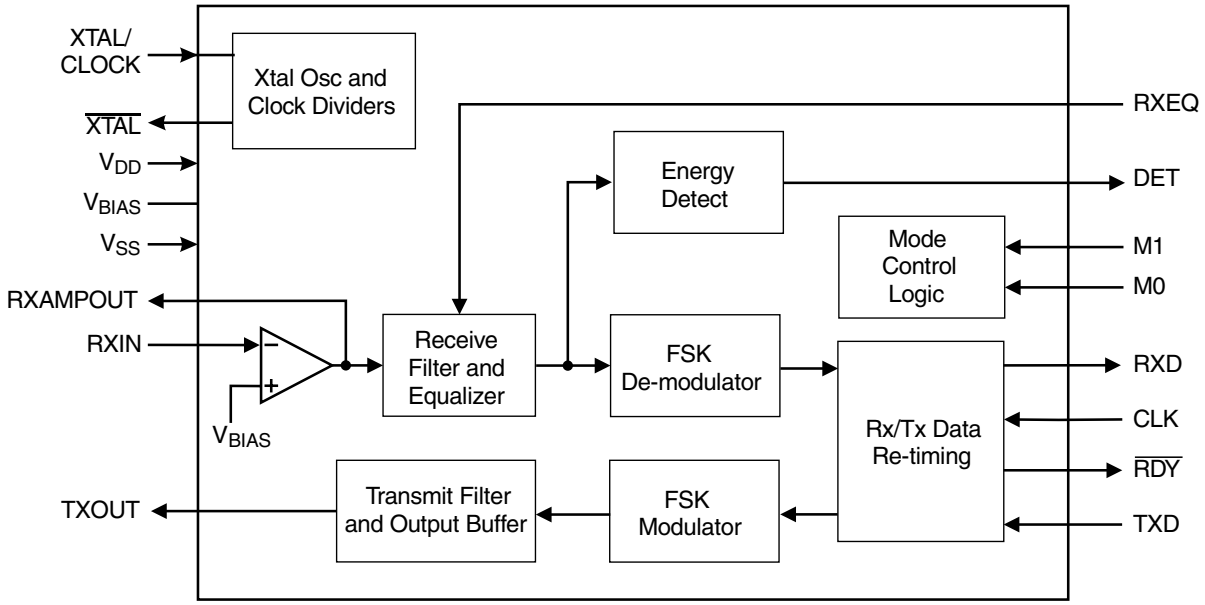
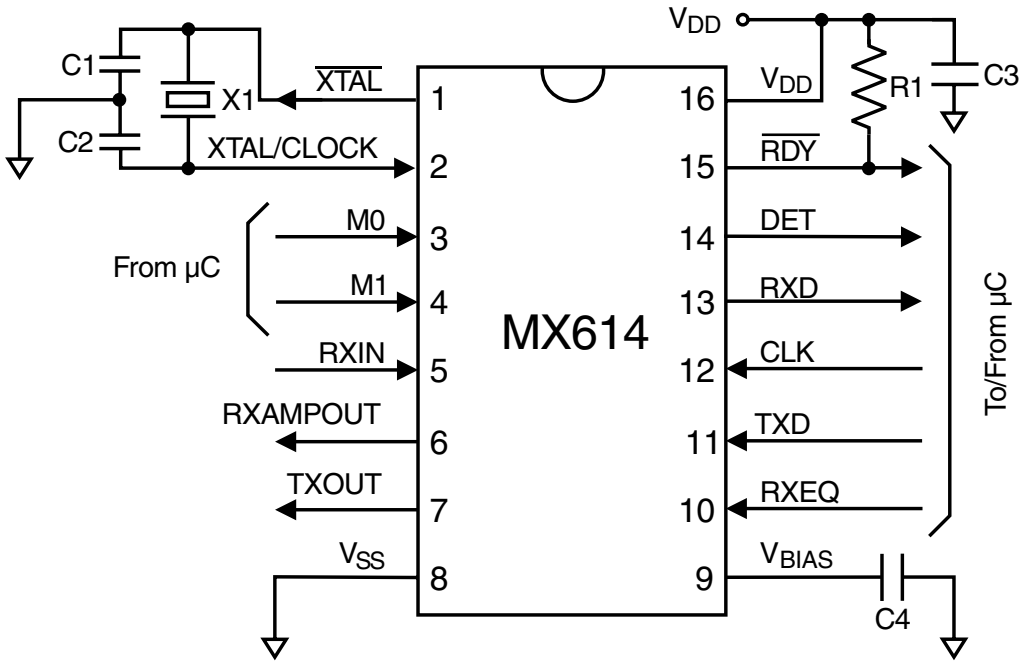


Figure 1: Block Diagram

2. Signal List

Pin No.		Signal		Description
P, DW	TN	Name	Type	
1	1	$\overline{XTAL}$	output	Output of the on-chip Xtal oscillator inverter.
2	2	XTAL/CLOCK	input	Input to the on-chip Xtal oscillator inverter.
3	5	M0	input	A logic level input for setting the mode of the device. See section 4.2
4	6	M1	input	A logic level input for setting the mode of the device. See section 4.2
5	7	RXIN	input	Input to the Rx input amplifier.
6	8	RXAMPOUT	output	Output of the Rx input amplifier
7	11	TXOUT	output	Output of the FSK generator.
8	12	V_{SS}	Power	Negative supply (ground).
9	13	V_{BIAS}	output	Internally generated bias voltage, held at $V_{DD}/2$ when the device is not in 'Zero-Power' mode. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
10	14	RXEQ	input	A logic level input for enabling/disabling the equalizer in the receive filter. See section 4.4
11	17	TXD	input	A logic level input for either the raw input to the FSK Modulator or data to be re-timed depending on the state of the M0, M1 and CLK inputs. See section 4.9
12	18	CLK	input	A logic level input which may be used to clock data bits in or out of the FSK Data Retiming block.
13	19	RXD	output	A logic level output carrying either the raw output of the FSK Demodulator or re-timed characters depending on the state of the M0, M1 and CLK inputs. See section 4.8
14	20	DET	output	A logic level output of the on-chip Energy Detect circuit.
15	23	$\overline{RDY}$	output	"Ready for data transfer" output of the on-chip data retiming circuit. This open-drain active low output may be used as an Interrupt Request/Wake-up input to the associated µC. An external pull-up resistor should be connected between this output and V_{DD}.
16	24	V_{DD}	Power	Positive supply. Levels and thresholds within the device are proportional to this voltage. Should be bypassed to V_{SS} by a capacitor mounted close to the device pins.
	3, 4, 9, 10, 15, 16, 21, 22	N/C		No internal connection

3. External Components



R1		100kΩ	±5%
C1 C2		18pF	±10%
C3		0.1µF	±10%
C4		0.1µF	±10%
X1	Note 1	3.579545MHz	

Figure 2: Recommended External Components for Typical Application

External Components Notes

1. **IMPORTANT:** This device is capable of detecting and decoding small amplitude signals. To achieve this V_{DD} and V_{BIAS} decoupling and protecting the receive path from extraneous in-band signals are very important. It is recommended that the decoupling capacitors be placed so that connections between them and the device pins are as short as practicable e.g. ≤ 1 inch from device pins. A ground plane protecting the receive path will help attenuate interfering signals
2. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD} peak-peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.

4. General Description

4.1 Xtal Osc and Clock Dividers

Frequency and timing accuracy of the MX614 is determined by a 3.579545MHz clock signal present at the XTAL/CLOCK pin. This may be generated by the on-chip oscillator inverter using the external components C1, C2 and X1 of Figure 2, or may be supplied from an external source to the XTAL/CLOCK input. If supplied from an external source, C1, C2 and X1 should not be fitted.

The on-chip oscillator is turned off in the 'Zero-Power' mode.

If the clock is provided by an external source which is not always running, then the 'Zero-Power' mode must be set when the clock is not available. Failure to observe this rule may cause a significant rise in the supply current drawn by MX614 as well as generating undefined states of the RXD, DET and $\overline{RDY}$ outputs.

4.2 Mode Control Logic

The MX614's operating mode is determined by the logic levels applied to the M0 and M1 input pins:

M1	M0	Rx Mode	Tx Mode	Data Retime[1]
0	0	1200bps	150bps	Rx
0	1	Off	1200bps	Tx
1	0	1200bps	Off / 5bps	Rx
1	1	'Zero-Power'		-

[1] If enabled

Note: On applying power to the device, the mode must be set to 'ZP', i.e. M0 = '1', M1 = '1', until V_{DD} has stabilized.

In the 'Zero-Power' (ZP) mode, power is removed from all internal circuitry. When leaving the 'ZP' mode there must be a delay of 20ms before any Tx data is passed to, or Rx data read from the device to allow the bias level, filters, and oscillator to stabilize.

4.3 Rx Input Amplifier

This amplifier is used to adjust the received signal to the correct amplitude for the FSK receiver and Energy Detect circuits (see section 5.1).

4.4 Receive Filter and Equalizer

The Receive Filter and Equalizer section is used to attenuate out of band noise and interfering signals, especially the locally generated transmit tones which might otherwise reach the 1200bps FSK Demodulator and Energy Detector circuits. This block also includes a switchable equalizer section. When the RXEQ pin is low, the overall group delay of the receive filter is flat over the 1200bps frequency range. If the RXEQ pin is high the receive filter's typical overall group delay will be as shown in Figure 3.

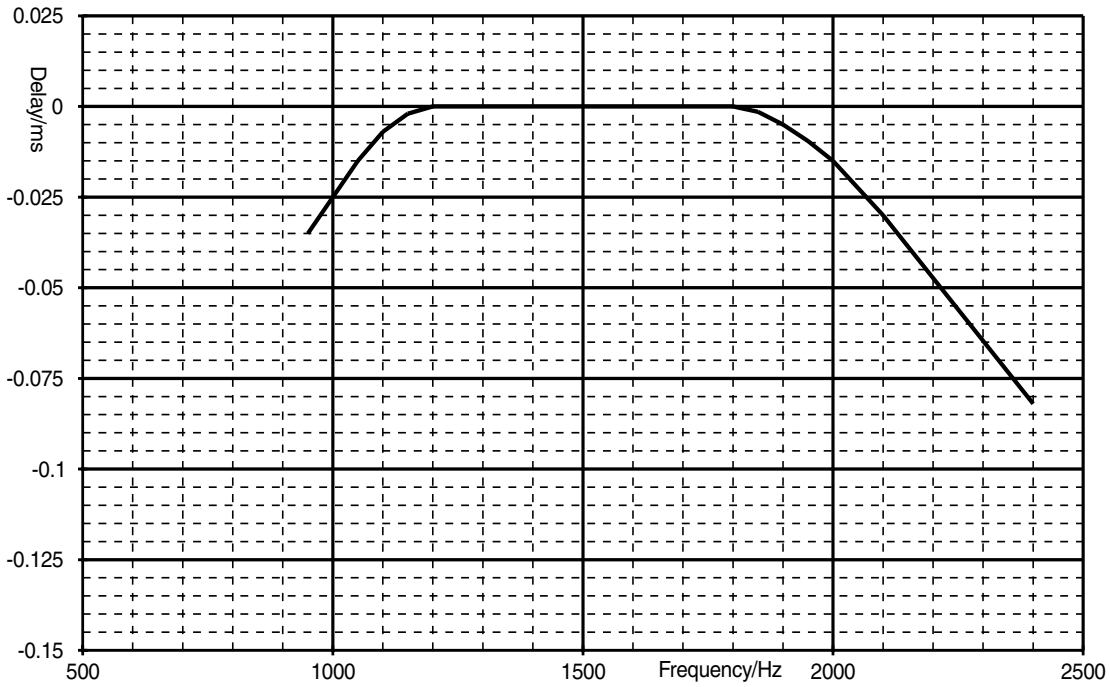


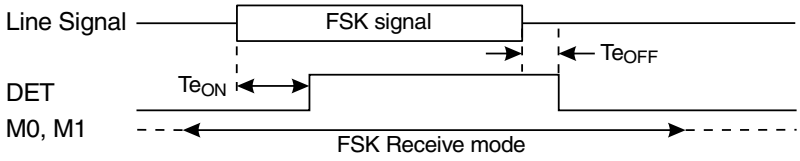
Figure 3: Rx Equalizer Group Delay (RXEQ = '1') wrt 1700Hz

4.5 Energy Detector

This block operates by measuring the level of the signal at the output of the Receive Filter, and comparing it against a preset threshold.

The DET output will be set high when the level has exceeded the threshold for a sufficient period of time. Amplitude and time hysteresis are used to reduce chattering of the DET output in marginal conditions.

Note that this circuit may also respond to non-FSK signals such as speech.



See section 6.1 for definitions of Te_{ON} and Te_{OFF}

Figure 4: FSK Level Detector Operation

4.6 FSK Demodulator

This block converts the 1200bps FSK input signal to a logic level received data signal which is output via the RXD pin as long as the Data Retiming function is not enabled (see section 4.8). This output does not depend on the state of the DET output.

When the Rx 1200bps mode is 'Off' or in 'ZP' the DET and RXD pins are held low.

Note that in the absence of a valid FSK signal, the demodulator may falsely interpret speech or other extraneous signals as data. For this reason it is advised that the RXD pin is read only when data is expected.

4.7 FSK Modulator and Transmit Filter

These blocks produce a tone according to the TXD, M0 and M1 inputs as shown in the table below, assuming data retiming is not being used:

M1	M0	TXD = 0	TXD = 1
1	1	-	-
1	0	0Hz[1]	387Hz
0	0	487Hz	387Hz
0	1	2200Hz	1200Hz

Note: [1] TXOUT held at approx. $V_{DD}/2$.

When modulated at the appropriate baud rates, the Transmit Filter and associated external components (see section 5.1) limit the FSK out of band energy sent to the line in accordance with Figure 5 and Figure 6, assuming that the signal on the line is at -6dBm or less.

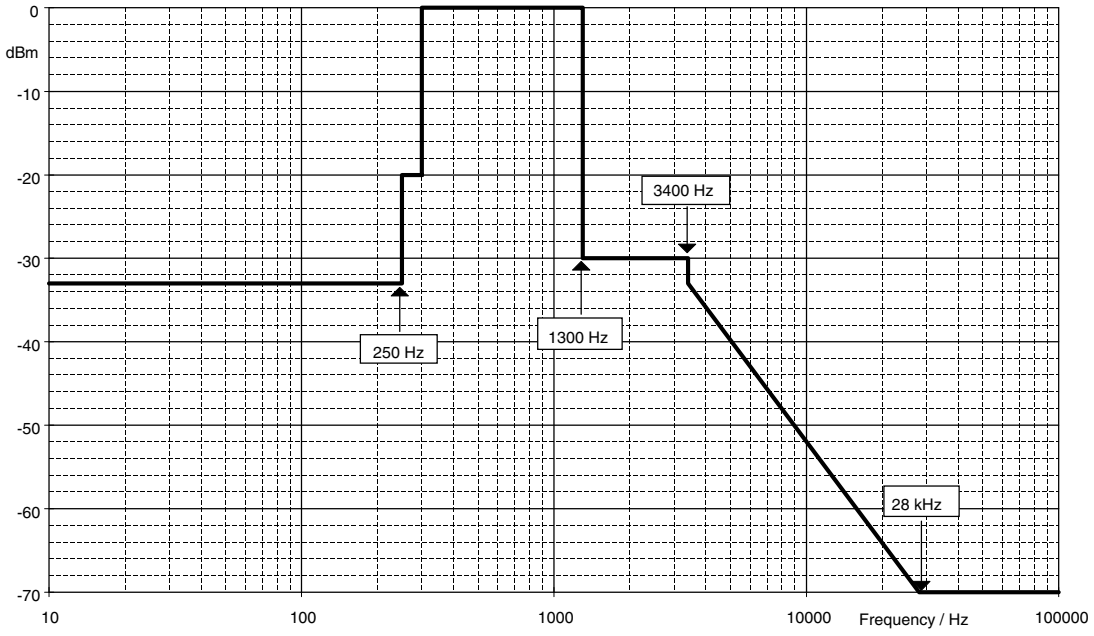


Figure 5: Tx limits at 5bps and 150bps rate

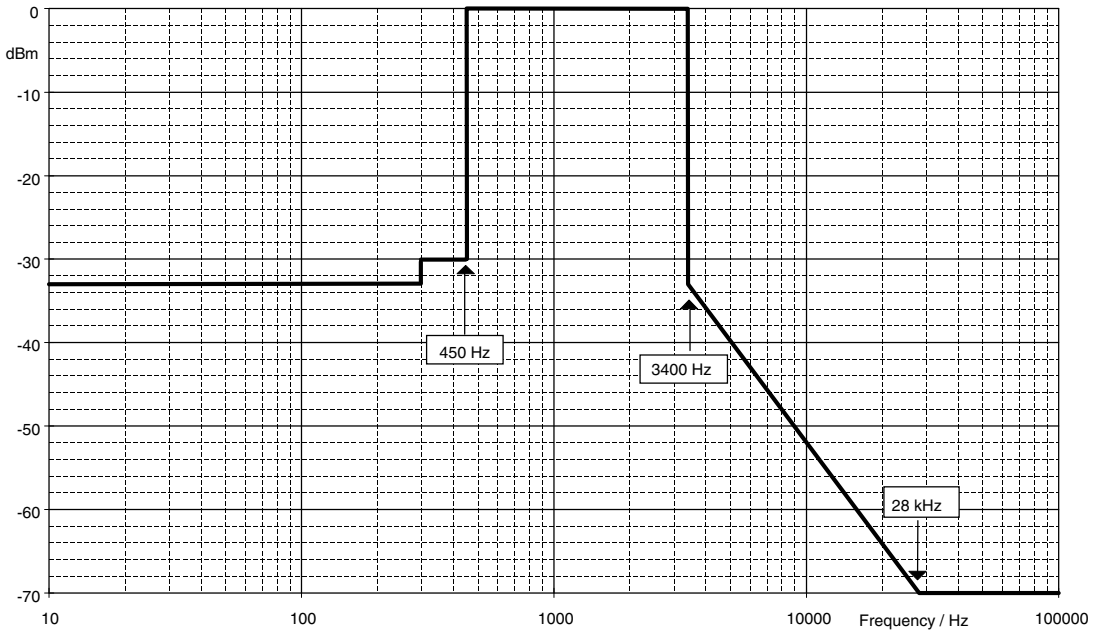


Figure 6: Tx limits at 1200bps rate

4.8 Rx Data Retiming

This function may be used when the received data consists of 1200bps asynchronous characters, each character consisting of one start bit followed by a minimum of 9 formatted bits as shown in the table below. **Note: Rx Data Retiming is not supported for data rates exceeding 1212bps.**

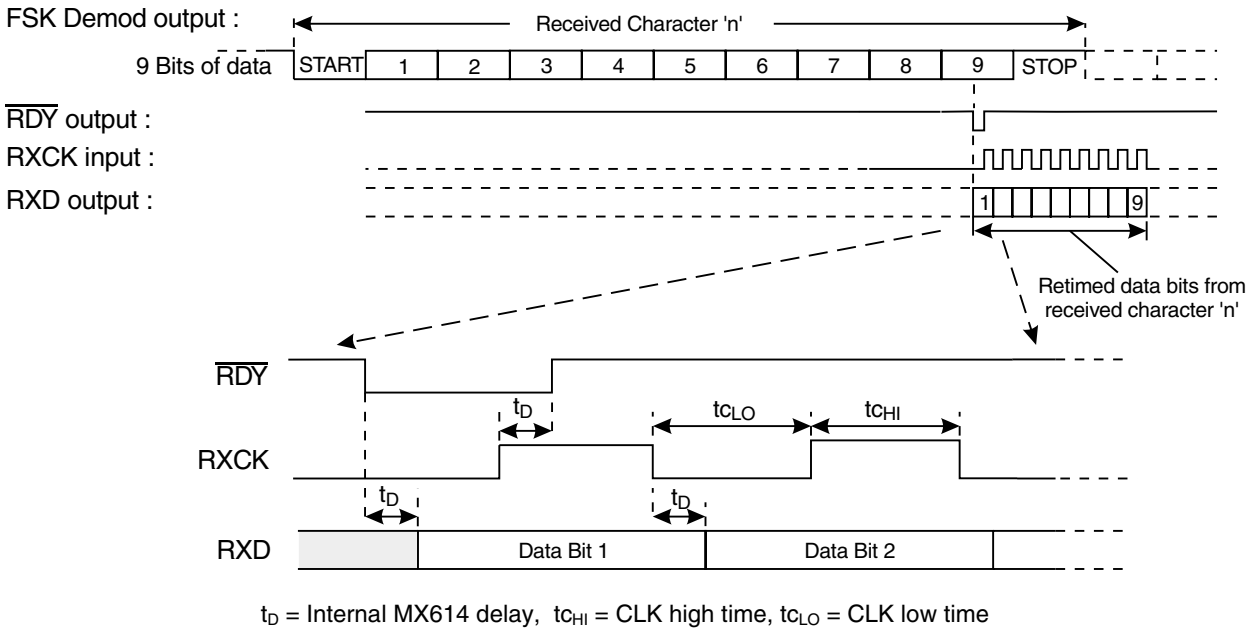
Data bits	Parity bits	Stop bits
7	0	≥ 2
7	1	≥ 1
8	0	≥ 1
8	1	≥ 1
9	0	≥ 1

The Data Retiming block, when enabled in receive mode, extracts the first 9 bits of each character following the start bit from the received asynchronous data stream, and presents them to the µC under the control of strobe pulses applied to the CLK input. The timing of these pulses is not critical and they may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The receive retiming block consists of two 9-bit shift registers, the input of the first is connected to the output of the FSK demodulator and the output of the second is connected to the RXD pin. The first register is clocked by an internally generated signal that stores the 9 received bits following the timing reference of a high to low transition at the output of the FSK demodulator. When the 9th bit is clocked into the first register these 9 bits are transferred to the second register, a new stop-start search is initiated and the CLK input is sampled. If the CLK input is low at this time the $\overline{\text{RDY}}$ pin is pulled low and the first received bit is output on the RXD pin. The CLK pin should then be pulsed high 9 times, the first 8 high to low transitions will be used by the device to clock out the bits in the second register. The $\overline{\text{RDY}}$ output is cleared the first time the CLK input goes high. At the end of the 9th pulse the RXD pin will be connected to the FSK demodulator output.

So to use the Data Retiming function, the CLK input should be kept low until the $\overline{\text{RDY}}$ output goes low; if the Data Retiming function is not required the CLK input should be kept high at all times.

The only restrictions on the timing of the CLK waveform are those shown in Figure 7 and the need to complete the transfer of all nine bits into the µC within the time of a complete character at 1200bps. See Section 6.2 for Timing specifications.



t_D = Internal MX614 delay, tc_{HI} = CLK high time, tc_{LO} = CLK low time

Figure 7: FSK Operation with Rx Data Retiming

Note that, if enabled, the Data Retiming block may interpret speech or other signals as random characters.

If the Data Retiming facility is not required, the CLK input to the MX614 should be kept high at all times. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the $\overline{RDY}$ output will not be activated by the FSK signal. This case is illustrated by the example in Figure 8.

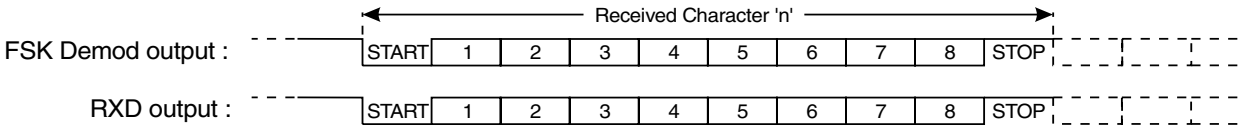


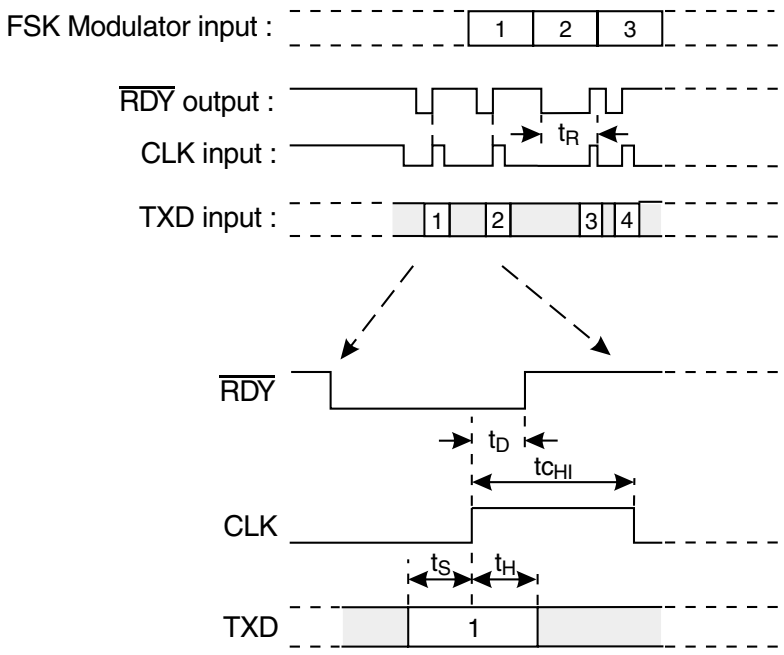
Figure 8: FSK Operation without Rx Data Retiming (CLK always high)

4.9 Tx Data Retiming

The Data Retiming block, when enabled in 1200bps transmit mode, requires the controlling µC to load one bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical and it may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead. **Note: Tx Data Retiming is not supported for data rates exceeding 1212bps.**

The Tx re-timing circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the $\overline{RDY}$ pin is pulled low. The $\overline{RDY}$ output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.

So to use the retiming option the CLK input should be held low until the $\overline{RDY}$ output is pulled low. When the $\overline{RDY}$ pin goes low the next data bit should be applied at the TXD input and the CLK input pulled high and then low within the time limits set out in Figure 9. See Section 6.2 for Timing specifications.



t_D = Internal MX614 delay, t_R = $\overline{RDY}$ low to CLK going low, t_S = data set up time

tc_{HI}= CLK high time, t_H = data hold time

Figure 9: FSK Operation with Tx Data Retiming

To ensure synchronization between the controlling device and the MX614 when entering Tx retiming mode the TXD pin must be held at a constant logic level from when the CLK pin is first pulled low to the end of loading in the second retimed bit. Similarly when exiting Tx retiming mode the TXD pin should be held at the same logic level as the last retimed bit for at least 2 bit times after the CLK line is pulled high.

If the data retiming facility is not required, the CLK input to the MX614 should be kept high at all times. The asynchronous data to the FSK modulator will then be connected directly to the TXD input pin. This is illustrated in Figure 10 and will also be the case when transmitting 5bps or 150bps data which has no retime option.

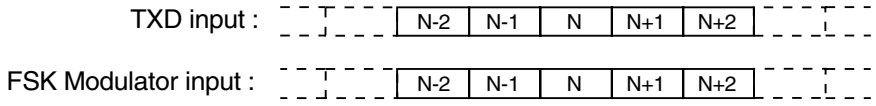


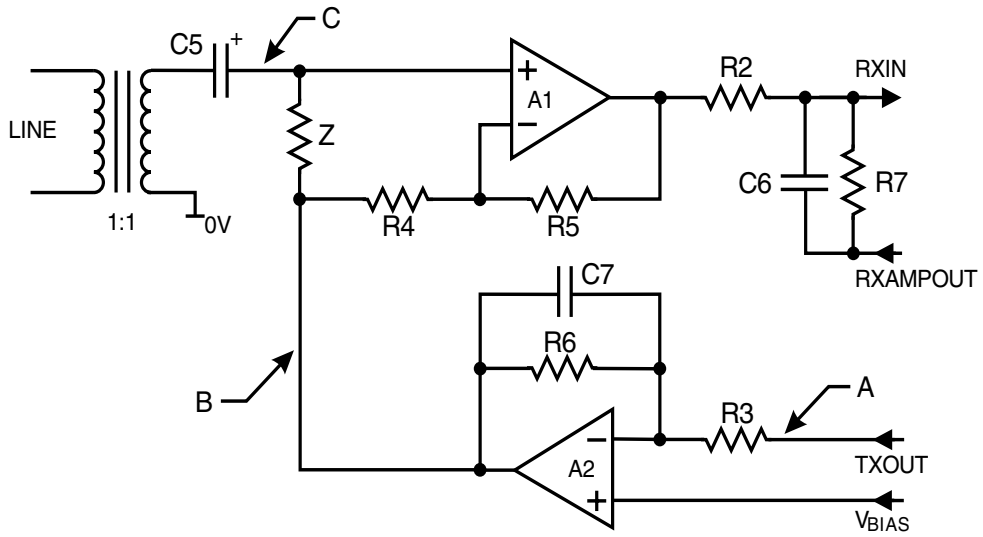
Figure 10: FSK Operation without Tx Data Retiming (CLK always high)

5. Application

5.1 Line Interface

The signals on the telephone line are not suitable for direct connection to the MX614. A Line Interface circuit is required to:

- Provide high voltage and dc isolation
- Attenuate the Tx signal present at the Rx input
- Provide the low impedance drive necessary for the line
- Filter the Tx and Rx signals



R2	See Notes		±1%,
R3	See Notes		±1%,
R4-R7		100kΩ	±1%,
C5		22µF	±20%
C6		100pF	±10%
C7		330pF	±10%

Figure 11: Line Interface Circuit

Line Interface Notes:

1. The components 'Z' between points B and C should match the line impedance.
2. Device A2 must be able to drive 'Z' and the line.
3. R2: For optimum results R2 should be set so that the gain is V_{DD}/5.0, i.e. R2 = 100kΩ at V_{DD} = 5.0V, rising to 150kΩ at V_{DD} = 3.3V.
4. R3: The levels in dB (relative to a 775mV_{RMS} signal) at 'A', 'B' and 'C' in the line interface circuit are:

Level at 'A' = 20Log(V_{DD}/5)
" 'B' = 'A' + 20Log(100kΩ/R3)
" 'C' = 'B' - 6

Example:

V_{DD}	'A'	R3	'B'	'C'
3.3V	-3.6dB	100kΩ	-3.6dB	-9.6dB
5.0V	0dB	150kΩ	-3.5dB	-9.5dB

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of and pins			
V_{DD}	-30	30	mA
V_{SS}	-30	30	mA
Any other pins	-20	20	mA
DW / PDIP Packages			
Total Allowable Power Dissipation at T_{AMB} = 25°C		800	mW
Derating above 25°C		13	mW/°C above 25°C
Storage Temperature	-55	125	°C
Operating Temperature	-40	85	°C

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		3.0	5.5	V
Operating Temperature		-40	85	°C
Xtal Frequency	1	3.575965	3.583125	MHz

Operating Limits Notes:

1. A crystal frequency of 3.579545MHz ±0.1% is required for correct FSK operation.

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 3.3V at T_{AMB} = 25°C
Xtal Frequency = 3.579545MHz ± 0.1% 0dBV corresponds to 1.0V_{RMS}
Tx and Rx data rates = 1200bps.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (M0 = '1', M1 = '1')	1, 2		1.0		µA
I_{DD} (M0 or M1 = '0') at V_{DD} = 3.0V	1		1.0	1.25	mA
I_{DD} (M0 or M1 = '0') at V_{DD} = 5.0V	1		1.7	2.5	mA
Logic '1' Input Level		70%			V_{DD}
Logic '0' Input Level				30%	V_{DD}
Logic Input Leakage Current (V_{IN} = 0 to V_{DD}), Excluding XTAL/CLOCK Input		-1.0		1.0	µA
Output Logic '1' Level (I_{OH} = 360µA)		V_{DD} -0.4			V
Output Logic '0' Level (I_{OL}= 360µA)				0.4	V
$\overline{RDY}$ Output 'off' State Current (V_{OUT} = V_{DD})				1.0	µA
FSK Demodulator					
Bit Rate	3	0	1200	1818	Baud
Mark (Logical '1') Frequency		1188	1200	1212	Hz
Space (Logical '0') Frequency		2178	2200	2222	Hz
Valid Input Level Range	4, 5	-40.0		-8.0	dBV
Maximum Twist (Mark Level wrt Space Level)		±6.0			dB
Acceptable Signal to Noise Ratio	6	20.0			dB
Level Detector 'On' Threshold Level	4			-40.0	dBV
Level Detector 'Off' to 'On' Time (Figure 4 Te_{ON})				25.0	ms
Level Detector 'On' to 'Off' Time (Figure 4 Te_{OFF})		8.0			ms
FSK Retiming					
Acceptable Rx Data Rate		1188	1200	1212	Baud
Tx Data Rate		1194		1206	Baud
FSK Modulator					
TXOUT Level Driving ≥ 40kΩ load	7	-3.2	-2.2	-1.2	dBV
Twist (Mark Level wrt Space Level)		-2.0	0	2.0	dB
Tx 1200bps (M1 = '0', M0 = '1').					
Bit Rate	3	0	1200	1818	Baud
Mark (Logical '1') Frequency		1197		1203	Hz
Space (Logical '0') Frequency		2196		2204	Hz
Tx 150bps (M1 = '0', M0 = '0').					
Bit Rate		0	150	152	Baud
Mark (Logical '1') Frequency		385		389	Hz
Space (Logical '0') Frequency		485		489	Hz
Tx 5bps (M1 = '1', M0 = '0').					
Bit Rate		0	5.0	5.1	Baud
Mark (Logical '1') Frequency		385		389	Hz

	Notes	Min.	Typ.	Max.	Units
Space (Logical '0') Frequency	8		0		Hz
Input Amplifier					
Impedance (RXIN Pin)	9	10.0			MΩ
Voltage Gain	9		500		V/V
XTAL/CLOCK Input					
'High' Pulse Width	10	100			ns
'Low' Pulse Width	10	100			ns

Operating Characteristics Notes:

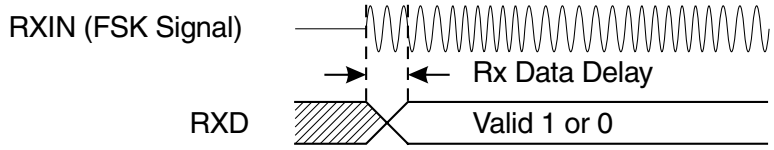
1. Not including any current drawn from the MX614 pins by external circuitry other than X1, C1 and C2.
2. TXD, RXEQ and CLK inputs at V_{SS}, M0 and M1 inputs at V_{DD}.
3. Tested at 1200bps.
4. Measured at the Rx Input Amplifier output (pin RXAMPOUT) for 1200Hz and V_{DD}= 5.0V. The internal threshold levels are proportional to V_{DD}. To cater for other supply voltages or different signal level ranges the voltage gain of the Rx Input Amplifier should be adjusted by selecting the appropriate external components as described in section 5.1.
5. Best 1818bps performance is achieved when the minimum Input Level is ≥ -32dBV.
6. Flat noise in 200 - 3200Hz band.
7. At V_{DD}= 5.0V. (-2.2dBV is equivalent to 0dBm ref. 775mV_{RMS} into 600Ω.)
8. TXOUT held at approximately V_{DD}/2.
9. Open loop, small signal low frequency measurements.
10. Timing for an external input to the XTAL/CLOCK pin.

6.2 Timing

Data and Mode Timing	Notes	Min.	Typ.	Max.	Units
Rx Data Delay (RXIN to RXD)	1, 5		2.55		ms
Tx Delay Data (TXD to TXOUT)	1, 6		0.1		ms
Mode change delay ZP to Tx or Rx	2			20	ms
Mode change delay Tx1200 to Rx1200	2			4.0	ms
Mode change delay Rx1200 to Tx1200	2			0.2	ms
t_D = Internal MX614 delay	3, 4			1	µs
tc_{HI} = CLK High time	3, 4	1			µs
tc_{LO} = CLK low time	3	1			µs
t_R = RDY low to CLK going low	4			800	µs
t_S = Data Set-up time	4	1			µs
t_H = Data Hold time	4	1			µs

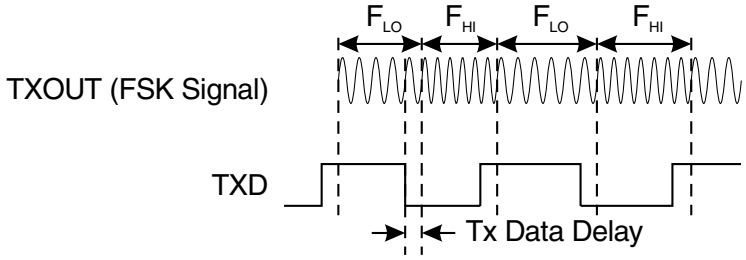
Timing Notes

1. When data retiming is not enabled.
2. Delay from mode change to reliable data at TXOUT or RXD pins.
3. Reference Figure 7.
4. Reference Figure 9.
5. Reference Figure 12.
6. Reference Figure 13.



Note: M0 and M1 are preset and stable.

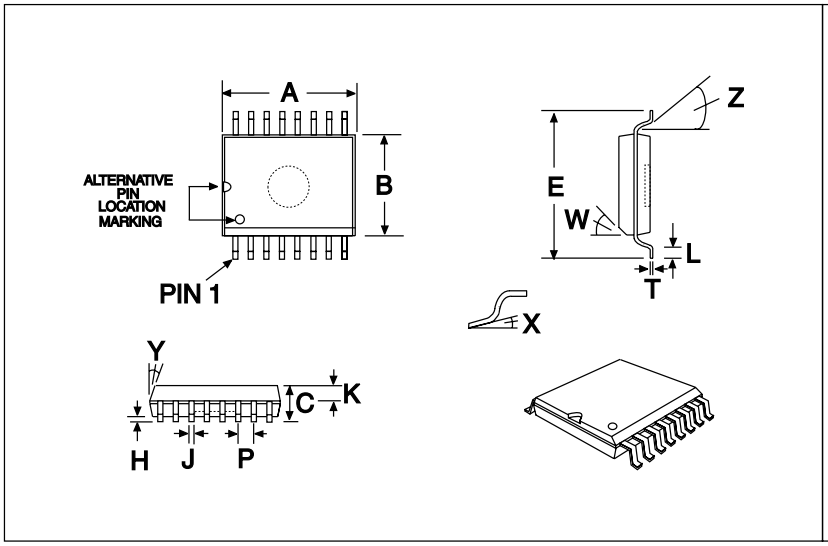
Figure 12: RXIN to RXD Delay time



Note: M0 and M1 are preset and stable. F_{LO} and F_{HI} are the two FSK signaling frequencies.

Figure 13: TXD to TXOUT Delay time

6.3 Packaging

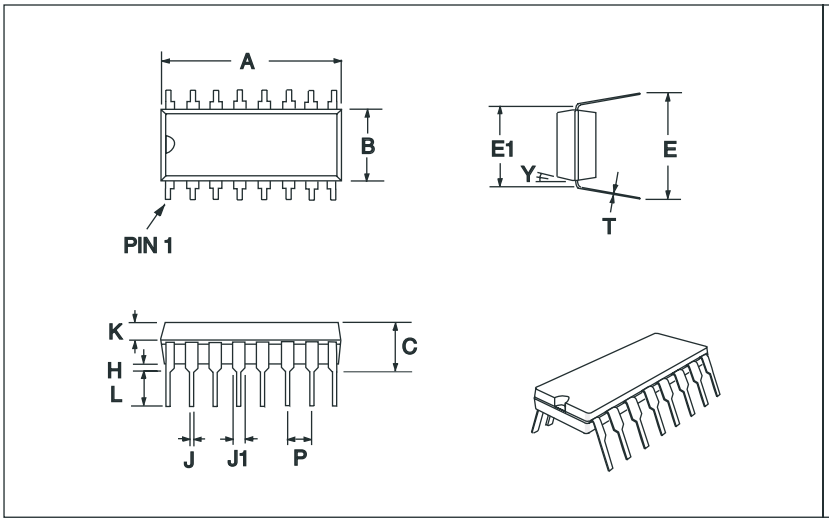


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.395 (10.03)		0.413 (10.49)
B	0.286 (7.26)		0.299 (7.59)
C	0.093 (2.36)		0.105 (2.67)
E	0.390 (9.90)		0.419 (10.64)
H	0.003 (0.08)		0.020 (0.51)
J	0.013 (0.33)		0.020 (0.51)
K		0.041 (1.04)	
L	0.016 (0.41)		0.050 (1.27)
P		0.050 (1.27)	
T	0.009 (0.23)		0.0125 (0.32)
W		45°	
X	0°		10°
Y	5°		7°
Z		5°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 14: 16-pin SOIC Mechanical Outline: *Order as part no. MX614DW*

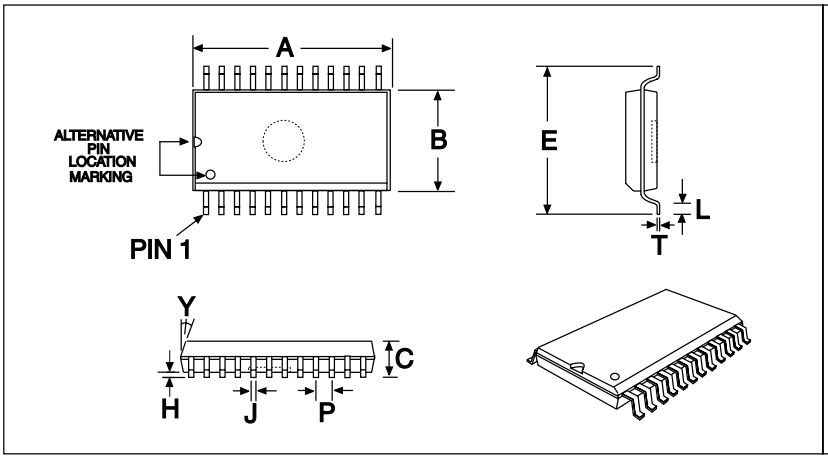


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.740 (18.80)		0.810 (20.57)
B	0.240 (6.10)		0.262 (6.63)
C	0.135 (3.43)		0.200 (5.06)
E	0.300 (7.62)		0.390 (9.91).
E1	0.290 (7.37)		0.325 (8.26)
H	0.015 (0.38)		0.070 (1.77)
J	0.014 (0.35)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.056 (1.42)		0.064 (1.63)
L	0.121 (3.07)		0.150 (3.81)
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 15: 16-pin PDIP Mechanical Outline: *Order as part no. MX614P*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.303 (7.70)		0.311 (7.90)
B	0.169 (4.30)		0.177 (4.50)
C	----------		0.047 (1.20)
E	0.248 (6.30)		0.256 (6.50)
H	0.002 (0.05)		0.006 (0.15)
J	0.007 (0.17)		0.012 (0.30)
L	0.020 (0.50)		0.030 (0.75)
P		0.0256 (0.65)	
T	0.003 (0.08)		0.008 (0.20)
Y	0°		8°

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 16 : 24-pin TSSOP Mechanical Outline: *Order as part no. MX614TN*

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the **'MX-COM'** textual logo is being replaced by a **'CML'** textual logo.

Company contact information is as below:

CML Microcircuits (UK) Ltd
COMMUNICATION SEMICONDUCTORS

Oval Park, Langford, Maldon,
Essex, CM9 6WG, England
Tel: +44 (0)1621 875500
Fax: +44 (0)1621 875600
uk.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (USA) Inc.
COMMUNICATION SEMICONDUCTORS

4800 Bethania Station Road,
Winston-Salem, NC 27105, USA
Tel: +1 336 744 5050,
0800 638 5577
Fax: +1 336 744 5054
us.sales@cmlmicro.com
www.cmlmicro.com

CML Microcircuits (Singapore) Pte Ltd
COMMUNICATION SEMICONDUCTORS

No 2 Kallang Pudding Road, 09-05/
06 Mactech Industrial Building,
Singapore 349307
Tel: +65 7450426
Fax: +65 7452917
sg.sales@cmlmicro.com
www.cmlmicro.com

D/CML (D)/2 May 2002

Isolated, Single-Channel RS-232 Line Driver/Receiver

Data Sheet

ADM3251E

FEATURES

- 2.5 kV fully isolated (power and data) RS-232 transceiver
- *iso*Power integrated, isolated dc-to-dc converter
- 460 kbps data rate
- 1 Tx and 1 Rx
- Meets EIA/TIA-232E specifications
- ESD protection on R_{IN} and T_{OUT} pins
  - ±8 kV: contact discharge
  - ±15 kV: air gap discharge
- 0.1 µF charge pump capacitors
- High common-mode transient immunity: >25 kV/µs
- Safety and regulatory approvals
  - UL recognition
    - 2500 V rms for 1 minute per UL 1577
  - VDE Certificate of Conformity
    - DIN EN 60747-5-2 (VDE 0884 Teil 2): 2003-01
  - CSA Component Acceptance Notice #5A
- Operating temperature range: −40°C to +85°C
- Wide body, 20-lead SOIC package

APPLICATIONS

- High noise data communications
- Industrial communications
- General-purpose RS232 data links
- Industrial/telecommunications diagnostic ports
- Medical equipment

FUNCTIONAL BLOCK DIAGRAM

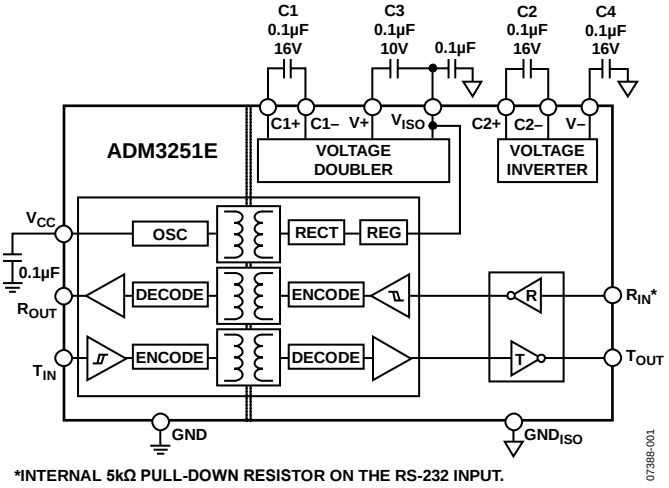


Figure 1.

GENERAL DESCRIPTION

The ADM3251E[1] is a high speed, 2.5 kV fully isolated, single-channel RS-232/V.28 transceiver device that operates from a single 5 V power supply. Due to the high ESD protection on the R_{IN} and T_{OUT} pins, the device is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently being plugged and unplugged.

The ADM3251E incorporates dual-channel digital isolators with *iso*Power™ integrated, isolated power. There is no requirement to use a separate isolated dc-to-dc converter. Chip-scale transformer *i*Coupler® technology from Analog Devices, Inc., is used both for the isolation of the logic signals as well as for the integrated dc-to-dc converter. The result is a total isolation solution.

The ADM3251E contains *iso*Power technology that uses high frequency switching elements to transfer power through the transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to Application Note AN-0971, *Control of Radiated Emissions with isoPower Devices*, for details on board layout considerations.

The ADM3251E conforms to the EIA/TIA-232E and ITU-T V. 28 specifications and operates at data rates up to 460 kbps.

Four external 0.1 µF charge pump capacitors are used for the voltage doubler/inverter, permitting operation from a single 5 V supply.

The ADM3251E is available in a 20-lead, wide body SOIC package and is specified over the −40°C to +85°C temperature range.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329.

Rev. G

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

ADM3251E* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADM3251E Evaluation board

DOCUMENTATION

Application Notes

- AN-740: iCoupler Isolation in RS-232 Applications

Data Sheet

- ADM3251E: Isolated, Single-Channel RS-232 Line Driver/ Receiver Data Sheet

User Guides

- UG-120: Standard Evaluation Kit User Guide for the ADM3251E
- UG-124: EMI optimized evaluation kit user guide for the ADM3251E
- UG-181: PLC Demo System, Industrial Process Control Demo System

REFERENCE MATERIALS

Press

- Analog Devices Achieves Major Milestone by Shipping 1 Billionth Channel of iCoupler Digital Isolation

Product Selection Guide

- Digital Isolator Product Selection and Resource Guide

Solutions Bulletins & Brochures

- RS-232 Transceivers Applications Bulletin (Summer 2008)

Technical Articles

- Inside iCoupler® Technology:ADuM347x PWM Controller and Transformer Driver with Quad-Channel Isolators Design Summary
- N*App*kin Note: Lowering the Power of the ADuM524x
- Part 1: Simplifying Design of Industrial Process-Control Systems with PLC Evaluation Boards
- Part 2: Simplifying Design of Industrial Process-Control Systems with PLC Evaluation Boards

DESIGN RESOURCES

- ADM3251E Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADM3251E EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

10/13—Rev. F to Rev. G

Added Patents Information, Note 1 ... 1
Changed Minimum External Tracking (Creepage) Value to 7.6 mm, Table 5 ... 5
Changes to Pin 9 Description and Pin 11 Descriptions, Table 8 ... 8
Changes to Isolation of Power and Data Section ... 11

6/12—Rev. E to Rev. F

Changes to Endnote 1 in Table 4 ... 5
Added DC Correctness and Magnetic Field Immunity Section ... 13
Added Figure 22 and Figure 23; Renumbered Sequentially ... 14
Updated Outline Dimensions and Changes to Ordering Guide ... 15

5/10—Rev. D to Rev. E

Changes to Features Section ... 1
Changes to Table 4 ... 5

3/10—Rev. C to Rev. D

Changes to Features and General Description Sections ... 1
Changes to Table 4 and Table 5 ... 5
Changed DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Insulation Characteristics (Pending) Heading to DIN EN 60747-5-2 (VDE 0884 Teil 2): 2003-01 Insulation Characteristics ... 6
Changes to Pollution Degree and Input–to-Output Test Voltage Parameters, Table 6 ... 6
Added Applications Information Section and Example PCB for Reduced EMI Section; Added Table 9 and Table 10; Renumbered Sequentially ... 13
Changes to PCB Layout Section ... 13
Added Isolated Power Supply Circuit Section, and Figure 22; Renumbered Sequentially ... 14

1/10—Rev. B to Rev. C

Changes to Table 4 ... 5

11/09—Rev. A to Rev. B

Changes to Figure 1 ... 1
Changed to Primary Side Supply Input Current, $I_{CC(DISABLE)}$ Maximum Limit to 2.5 mA ... 4
Changes to Table 4 ... 5
Changes to Figure 13 ... 11

9/08—Rev. 0 to Rev. A

Changes to Timing Parameters in Table 1 ... 3
Changes to Timing Parameters in Table 2 ... 4
Changes to Ordering Guide ... 14

7/08—Revision 0: Initial Version

SPECIFICATIONS

All voltages are relative to their respective ground; all minimum/maximum specifications apply over the entire recommended operating range; T_A = 25°C and V_{CC} = 5.0 V (dc-to-dc converter enabled), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC CHARACTERISTICS					
V_{CC} Operating Voltage Range	4.5		5.5	V	
DC-to-DC Converter Enable Threshold, $V_{CC(ENABLE)}$[1]	4.5			V	
DC-to-DC Converter Disable Threshold, $V_{CC(DISABLE)}$[1]			3.7	V	
DC-to-DC Converter Enabled					
Input Supply Current, $I_{CC(ENABLE)}$			110	mA	V_{CC} = 5.5 V, no load
			145	mA	V_{CC} = 5.5 V, R_L = 3 kΩ
V_{ISO} Output[2]		5.0		V	I_{ISO} = 0 µA
LOGIC					
Transmitter Input, T_{IN}					
Logic Input Current, I_{TIN}	−10	+0.01	+10	µA	
Logic Low Input Threshold, V_{TINL}			0.3 V_{CC}	V	
Logic High Input Threshold, V_{TINH}	0.7 V_{CC}			V	
Receiver Output, R_{OUT}					
Logic High Output, V_{ROUTH}	V_{CC} − 0.1	V_{CC}		V	I_{ROUTH} = −20 µA
	V_{CC} − 0.5	V_{CC} − 0.3		V	I_{ROUTH} = −4 mA
Logic Low Output, V_{ROUTL}		0.0	0.1	V	I_{ROUTH} = 20 µA
		0.3	0.4	V	I_{ROUTH} = 4 mA
RS-232					
Receiver, R_{IN}					
EIA-232 Input Voltage Range[3]	−30		+30	V	
EIA-232 Input Threshold Low	0.6	2.0		V	
EIA-232 Input Threshold High		2.1	2.4	V	
EIA-232 Input Hysteresis		0.1		V	
EIA-232 Input Resistance	3	5	7	kΩ	
Transmitter, T_{OUT}					
Output Voltage Swing (RS-232)	±5	±5.7		V	R_L = 3 kΩ to GND
Transmitter Output Resistance	300			Ω	V_{ISO} = 0 V
Output Short-Circuit Current (RS-232)		±12		mA	
TIMING CHARACTERISTICS					
Maximum Data Rate	460			kbps	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 1000 pF
Receiver Propagation Delay					
t_{PHL}		190		ns	
t_{PLH}		135		ns	
Transmitter Propagation Delay		650		ns	R_L = 3 kΩ, C_L = 1000 pF
Transmitter Skew		80		ns	
Receiver Skew		70		ns	
Transition Region Slew Rate[3]	5.5	10	30	V/µs	+3 V to −3 V or −3 V to +3 V, V_{CC} = +3.3 V, R_L = 3 kΩ, C_L = 1000 pF, T_A = 25°C
AC SPECIFICATIONS					
Output Rise/Fall Time, t_R/t_F (10% to 90%)		2.3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[4]	25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[4]	25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V
ESD PROTECTION (R_{IN} And T_{OUT} PINS)		±15		kV	Human body model air discharge
		±8		kV	Human body model contact discharge

[1] Enable/disable threshold is the V_{CC} voltage at which the internal dc-to-dc converter is enabled/disabled.
[2] To maintain data sheet specifications, do not draw current from V_{ISO}.
[3] Guaranteed by design.
[4] V_{CM} is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

All voltages are relative to their respective ground; all minimum/maximum specifications apply over the entire recommended operating range; T_A = 25°C, V_{CC} = 3.3 V (dc-to-dc converter disabled), and the secondary side is powered externally by V_{ISO} = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC CHARACTERISTICS					
V_{CC} Operating Voltage Range	3.0		3.7	V	
DC-to-DC Converter Disable Threshold, $V_{CC(DISABLE)}$ [1]			3.7	V	
DC-to-DC Converter Disabled					
V_{ISO} [2]	3.0		5.5	V	
Primary Side Supply Input Current, $I_{CC(DISABLE)}$			2.5	mA	No load
Secondary Side Supply Input Current, $I_{ISO(DISABLE)}$			12	mA	V_{ISO} = 5.5 V, R_L = 3 kΩ
Secondary Side Supply Input Current, $I_{ISO(DISABLE)}$		6.2		mA	R_L = 3 kΩ
LOGIC					
Transmitter Input, T_{IN}					
Logic Input Current, I_{TIN}	−10	+0.01	+10	µA	
Logic Low Input Threshold, V_{TINL}			0.3 V_{CC}	V	
Logic High Input Threshold, V_{TINH}	0.7 V_{CC}			V	
Receiver Output, R_{OUT}					
Logic High Output, V_{ROUTH}	V_{CC} − 0.1	V_{CC}		V	I_{ROUTH} = −20 µA
	V_{CC} − 0.5	V_{CC} − 0.3		V	I_{ROUTH} = −4 mA
Logic Low Output, V_{ROUTL}		0.0	0.1	V	I_{ROUTH} = 20 µA
		0.3	0.4		I_{ROUTH} = 4 mA
RS-232				V	
Receiver, R_{IN}					
EIA-232 Input Voltage Range [3]	−30		+30	V	
EIA-232 Input Threshold Low	0.6	1.3		V	
EIA-232 Input Threshold High		1.6	2.4	V	
EIA-232 Input Hysteresis		0.3		V	
EIA-232 Input Resistance	3	5	7	kΩ	
Transmitter, T_{OUT}					
Output Voltage Swing (RS-232)	±5	±5.7		V	R_L = 3 kΩ to GND
Transmitter Output Resistance	300			Ω	V_{ISO} = 0 V
Output Short-Circuit Current (RS-232)		±11		mA	
TIMING CHARACTERISTICS					
Maximum Data Rate	460			kbps	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 1000 pF
Receiver Propagation Delay					
t_{PHL}		190		ns	
t_{PLH}		135		ns	
Transmitter Propagation Delay		650		ns	R_L = 3 kΩ, C_L = 1000 pF
Transmitter Skew		80		ns	
Receiver Skew		55		ns	
Transition Region Slew Rate [3]	5.5	10	30	V/µs	+3 V to −3 V or −3 V to +3 V, V_{CC} = 3.3 V, R_L = 3 kΩ, C_L = 1000 pF, T_A = 25°C
AC SPECIFICATIONS					
Output Rise/Fall Time, t_R/t_F (10% to 90%)		2.3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output [4]	25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output [4]	25			kV/µs	V_{CM} = 1 kV, transient magnitude = 800 V
ESD PROTECTION (R_{IN} AND T_{OUT} PINS)		±15		kV	Human body model air discharge
		±8		kV	Human body model contact discharge

[1] Enable/disable threshold is the V_{CC} voltage at which the internal dc-to-dc converter is enabled/disabled.
[2] To maintain data sheet specifications, do not draw current from V_{ISO}.
[3] Guaranteed by design.
[4] V_{CM} is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-to-Output)	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Air Thermal Resistance	θ_{JA}		47.05		°C/W	

REGULATORY INFORMATION

Table 4.

UL[1]	VDE[2]	CSA
Recognized under 1577 Component Recognition Program File E214100	Certified according to DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01 File 2471900-4880-0001/123328	Approved under CSA Component Acceptance Notice #5A Basic Insulation per CSA 60950-1-07 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage File 2268268

[1] In accordance with UL 1577, each ADM3251E is proof tested by applying an insulation test voltage ≥3000 V rms for 1 sec (current leakage detection limit = 6 μA).
[2] Each ADM3251E is proof tested by applying an insulation test voltage ≥4000 V peak for 1 sec (partial discharge detection limit = 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.7	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		
Maximum Working Voltage Compatible with 50-Year Service Life	V_{IORM}	425	V peak	Continuous peak voltage across the isolation barrier

DIN EN 60747-5-2 (VDE 0884 TEIL 2): 2003-01 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

Table 6.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree			2	
Maximum Working Insulation Voltage		V_{IORM}	424	V peak
Input-to-Output Test Voltage				
Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	795	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure			
Case Temperature		T_S	150	°C
Supply Current		I_{S1}	531	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
V_{CC}, V_{ISO}	−0.3 V to +6 V
V+	(V_{CC} − 0.3 V) to +13 V
V−	−13 V to +0.3 V
Input Voltages	
T_{IN}	−0.3 V to (V_{CC} + 0.3 V)
R_{IN}	±30 V
Output Voltages	
T_{OUT}	±15 V
R_{OUT}	−0.3 V to (V_{CC} + 0.3 V)
Short-Circuit Duration	
T_{OUT}	Continuous
Power Dissipation	
θ_{JA}, Thermal Impedance	47.05°C/W
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature (Soldering, 30 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

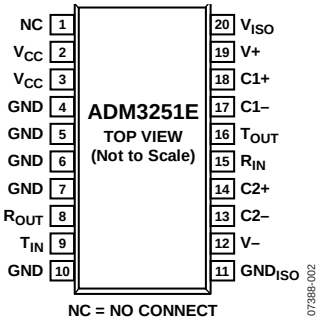


Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. This pin should always remain unconnected.
2, 3	V_{CC}	Power Supply Input. A 0.1 µF decoupling capacitor is required between V_{CC} and ground. When a voltage between 4.5 V and 5.5 V is applied to the V_{CC} pin, the integrated dc-to-dc converter is enabled. If this voltage is lowered to between 3.0 V and 3.7 V, the integrated dc-to-dc converter is disabled.
4, 5, 6, 7, 10	GND	Ground.
8	R_{OUT}	Receiver Output. This pin outputs CMOS logic levels.
9	T_{IN}	Transmitter (Driver) Input. This pin accepts CMOS levels.
11	GND_{ISO}	Ground Reference for Isolated RS-232 Side.
12	V–	Internally Generated Negative Supply.
13, 14	C2–, C2+	Positive and Negative Connections for Charge Pump Capacitors. External Capacitor C2 is connected between these pins; a 0.1 µF capacitor is recommended, but larger capacitors up to 10 µF can be used.
15	R_{IN}	Receiver Input. This input accepts RS-232 signal levels.
16	T_{OUT}	Transmitter (Driver) Output. This outputs RS-232 signal levels.
17, 18	C1–, C1+	Positive and Negative Connections for Charge Pump Capacitors. External Capacitor C1 is connected between these pins; a 0.1 µF capacitor is recommended, but larger capacitors up to 10 µF can be used.
19	V+	Internally Generated Positive Supply.
20	V_{ISO}	Isolated Supply Voltage for Isolator Secondary Side. A 0.1 µF decoupling capacitor is required between V_{ISO} and ground. When the integrated dc-to-dc converter is enabled, the V_{ISO} pin should not be used to power external circuitry. If the integrated dc-to-dc converter is disabled, power the secondary side by applying a voltage in the range of 3.0 V to 5.5 V to this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

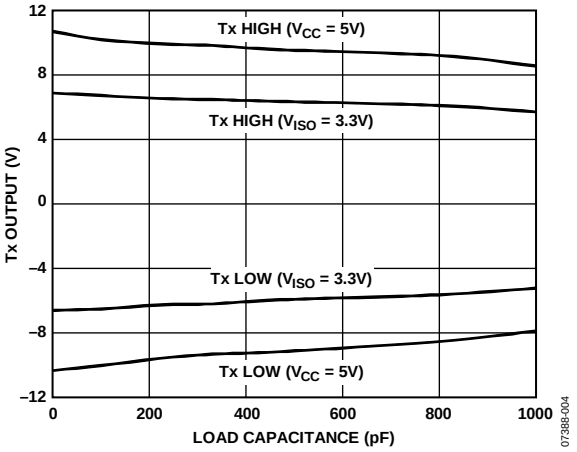


Figure 3. Transmitter Output Voltage High/Low vs. Load Capacitance at 460 kbps

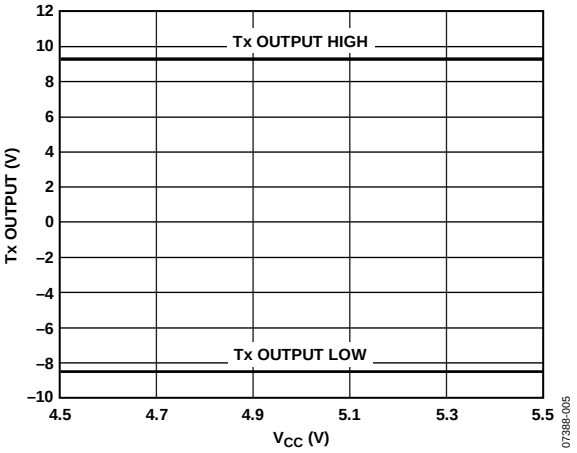


Figure 4. Transmitter Output Voltage High/Low vs. V_{CC}, R_L = 3 kΩ

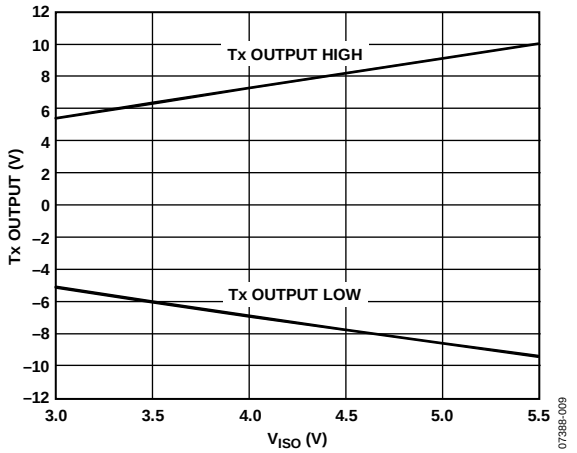


Figure 5. Transmitter Output Voltage High/Low vs. V_{ISO}, R_L = 3 kΩ

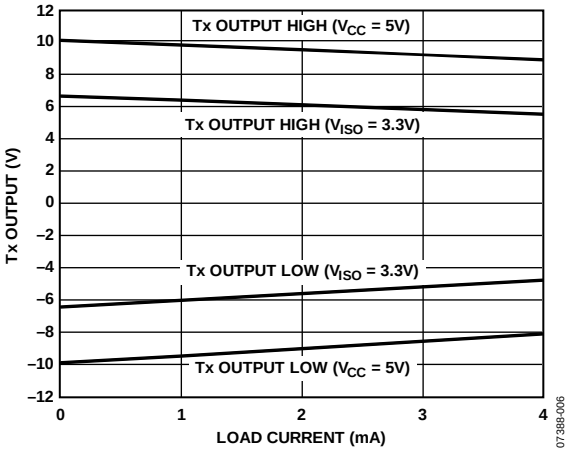


Figure 6. Transmitter Output Voltage High/Low vs. Load Current

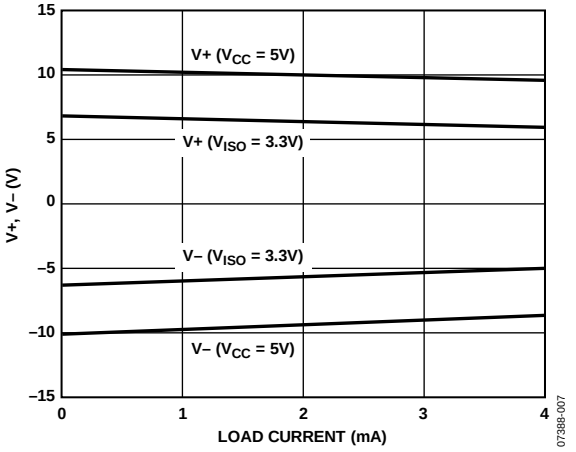


Figure 7. Charge Pump V+, V– vs. Load Current

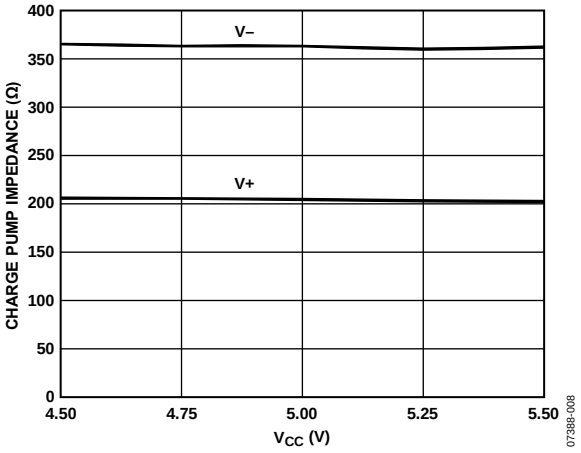


Figure 8. Charge Pump Impedance vs. V_{CC}

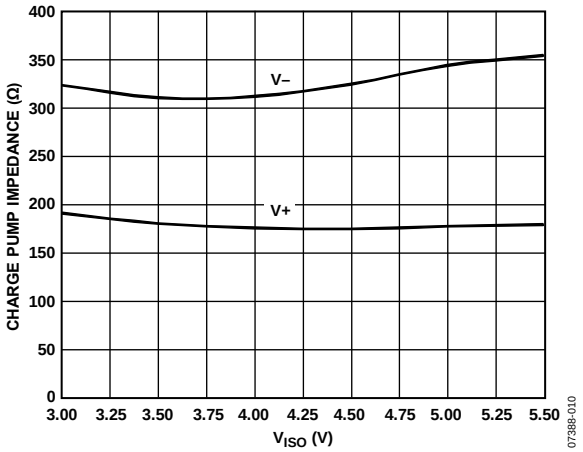


Figure 9. Charge Pump Impedance vs. V_{ISO}

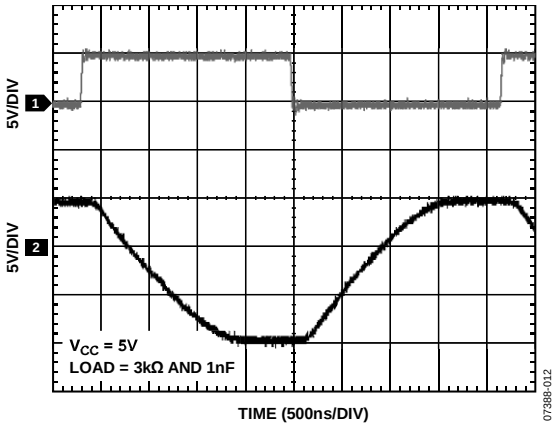


Figure 11. 460 kbps Data Transmission

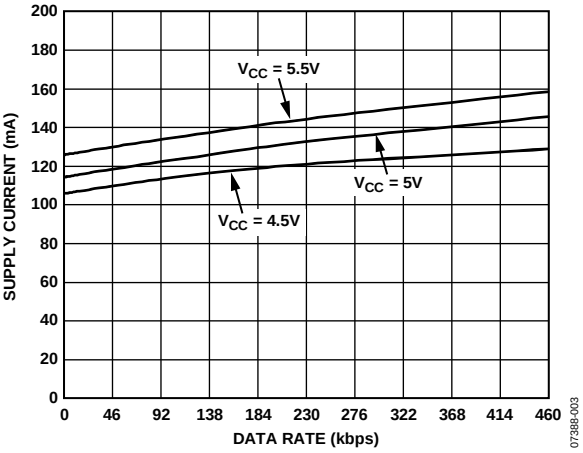


Figure 10. Primary Supply Current vs. Data Rate

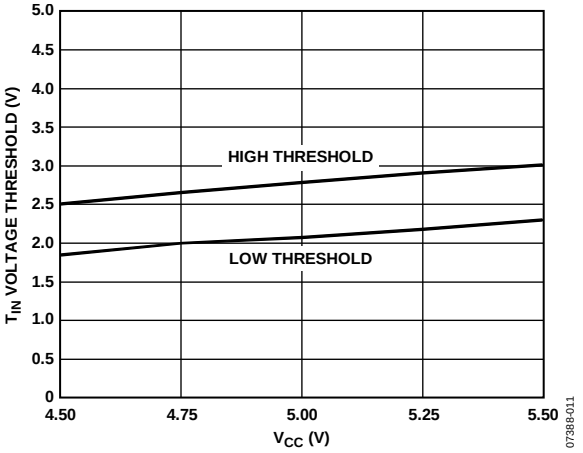


Figure 12. T_{IN} Voltage Threshold vs. V_{CC}

THEORY OF OPERATION

The ADM3251E is a high speed, 2.5 kV fully isolated, single-channel RS-232 transceiver device that operates from a single power supply.

The internal circuitry consists of the following main sections:

- Isolation of power and data
- A charge pump voltage converter
- A 5.0 V logic to EIA/TIA-232E transmitter
- A EIA/TIA-232E to 5.0 V logic receiver

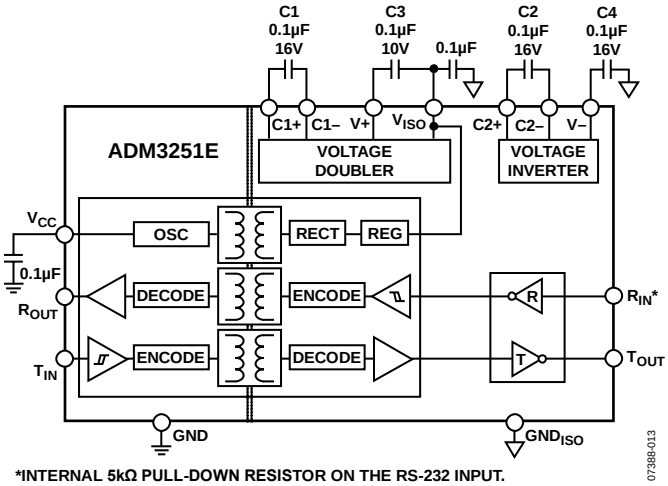


Figure 13. Functional Block Diagram

ISOLATION OF POWER AND DATA

The ADM3251E incorporates a dc-to-dc converter section, which works on principles that are common to most modern power supply designs. V_{CC} power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. Power is transferred to the secondary side, where it is rectified to a high dc voltage. The power is then linearly regulated to about 5.0 V and supplied to the secondary side data section and to the V_{ISO} pin. The V_{ISO} pin should not be used to power external circuitry.

Because the oscillator runs at a constant high frequency independent of the load, excess power is internally dissipated in the output voltage regulation process. Limited space for transformer coils and components also adds to internal power dissipation. This results in low power conversion efficiency.

The ADM3251E can be operated with the dc-to-dc converter enabled or disabled. The internal dc-to-dc converter state of the ADM3251E is controlled by the input V_{CC} voltage. In normal operating mode, V_{CC} is set between 4.5 V and 5.5 V and the internal dc-to-dc converter is enabled. To disable the dc-to-dc converter, lower V_{CC} to a value between 3.0 V and 3.7 V. In this mode, the user must externally supply isolated power to the V_{ISO} pin. An isolated secondary side voltage of between 3.0 V and 5.5 V and a secondary side input current, I_{ISO}, of 12 mA (maximum) is required on the V_{ISO} pin. The signal channels of the ADM3251E then continue to operate normally.

The T_{IN} pin accepts CMOS input levels (and TTL levels at V_{CC} = 3.3 V). The driver input signal that is applied to the T_{IN} pin is referenced to logic ground (GND). It is coupled across the isolation barrier, inverted, and then appears at the transceiver section, referenced to isolated ground (GND_{ISO}). Similarly, the receiver input (R_{IN}) accepts RS-232 signal levels that are referenced to isolated ground. The R_{IN} input is inverted and coupled across the isolation barrier to appear at the R_{OUT} pin, referenced to logic ground.

The digital signals are transmitted across the isolation barrier using *i*Coupler technology. Chip-scale transformer windings couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer of the winding. At the secondary winding, the induced waveforms are decoded into the binary value that was originally transmitted.

There is hysteresis in the V_{CC} input voltage detect circuit. Once the dc-to-dc converter is active, the input voltage must be decreased below the turn-on threshold to disable the converter. This feature ensures that the converter does not go into oscillation due to noisy input power.

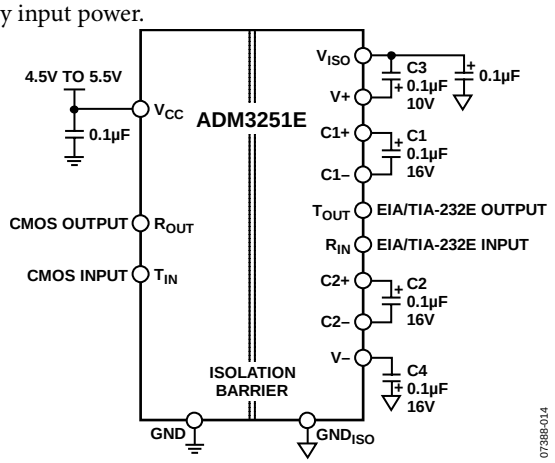


Figure 14. Typical Operating Circuit with the DC-to-DC Converter Enabled (V_{CC} = 4.5 V to 5.5 V)

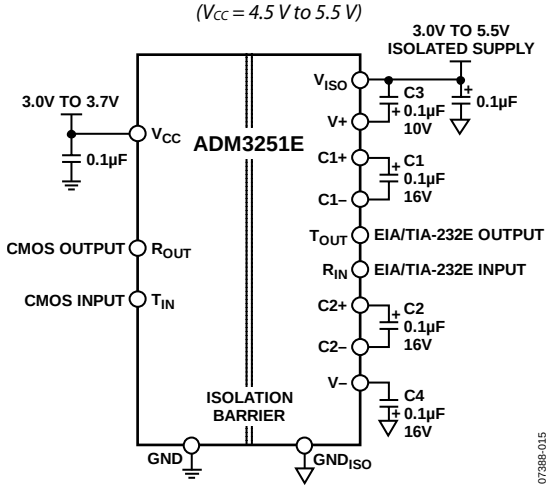


Figure 15. Typical Operating Circuit with the DC-to-DC Converter Disabled (V_{CC} = 3.0 V to 3.7 V)

CHARGE PUMP VOLTAGE CONVERTER

The charge pump voltage converter consists of a 200 kHz oscillator and a switching matrix. The converter generates a ±10.0 V supply from the input 5.0 V level. This is done in two stages by using a switched capacitor technique as illustrated in Figure 16 and Figure 17. First, the 5.0 V input supply is doubled to 10.0 V by using C1 as the charge storage element. The +10.0 V level is then inverted to generate −10.0 V using C2 as the storage element. C3 is shown connected between V+ and V_{ISO}, but is equally effective if connected between V+ and GND_{ISO}.

Capacitor C3 and Capacitor C4 are used to reduce the output ripple. Their values are not critical and can be increased, if desired. Larger capacitors (up to 10 µF) can be used in place of C1, C2, C3, and C4.

5.0 V LOGIC TO EIA/TIA-232E TRANSMITTER

The transmitter driver converts the 5.0 V logic input levels into RS-232 output levels. When driving an RS-232 load with V_{CC} = 5.0 V, the output voltage swing is typically ±10 V.

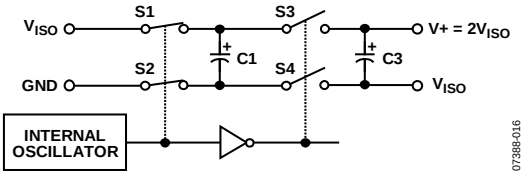


Figure 16. Charge Pump Voltage Doubler

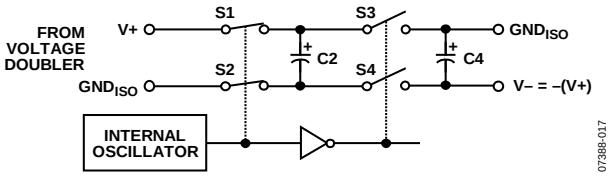


Figure 17. Charge Pump Voltage Inverter

EIA/TIA-232E TO 5 V LOGIC RECEIVER

The receiver is an inverting level-shifter that accepts the RS-232 input level and translates it into a 5.0 V logic output level. The input has an internal 5 kΩ pull-down resistor to ground and is also protected against overvoltages of up to ±30 V. An unconnected input is pulled to 0 V by the internal 5 kΩ pull-down resistor. This, therefore, results in a Logic 1 output level for an unconnected input or for an input connected to GND. The receiver has a Schmitt-trigger input with a hysteresis level of 0.1 V. This ensures error-free reception for both a noisy input and for an input with slow transition times.

HIGH BAUD RATE

The ADM3251E offers high slew rates, permitting data transmission at rates well in excess of the EIA/TIA-232E specifications. The RS-232 voltage levels are maintained at data rates up to 460 kbps.

THERMAL ANALYSIS

Each ADM3251E device consists of three internal die, attached to a split-paddle lead frame. For the purposes of thermal analysis, it is treated as a thermal unit with the highest junction temperature reflected in the θ_{JA} value from Table 7. The value of θ_{JA} is based on measurements taken with the part mounted on a JEDEC standard 4-layer PCB with fine-width traces in still air. Following the recommendations in the PCB Layout section decreases the thermal resistance to the PCB, allowing increased thermal margin at high ambient temperatures.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADM3251E.

The insulation lifetime of the ADM3251E depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 18, Figure 19, and Figure 20 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower.

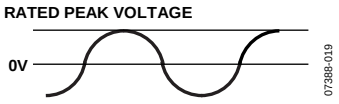


Figure 18. Bipolar AC Waveform

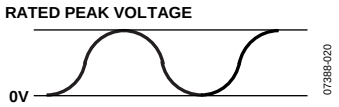


Figure 19. Unipolar AC Waveform

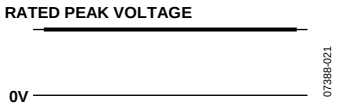


Figure 20. DC Waveform Outline Dimensions

APPLICATIONS INFORMATION

PCB LAYOUT

The ADM3251E requires no external circuitry for its logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 21). Bypass capacitors are conveniently connected between Pin 3 and Pin 4 for V_{CC} and between Pin 19 and Pin 20 for V_{ISO}. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

Because it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipating into the PCB through the ground pins. If the device is used at high ambient temperatures, care should be taken to provide a thermal path from the ground pins to the PCB ground plane. The board layout in Figure 21 shows enlarged pads for Pin 4, Pin5, Pin 6, Pin 7, Pin 10, and Pin 11. Multiple vias should be implemented from each of the pads to the ground plane, which significantly reduce the temperatures inside the chip. The dimensions of the expanded pads are left to the discretion of the designer and the available board space.

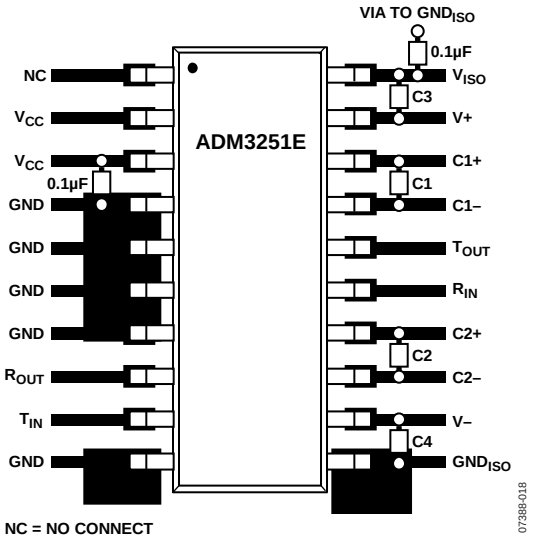


Figure 21. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side.

The power supply section of the ADM3251E uses a 300 MHz oscillator frequency to pass power through its chip-scale transformers. Operation at these high frequencies may raise concerns about radiated emissions and conducted noise. PCB layout and construction is a very important tool for controlling radiated emissions. Refer to Application Note AN-0971, *Control of Radiated Emissions with isoPower Devices*, for extensive guidance on radiation mechanisms and board layout considerations.

EXAMPLE PCB FOR REDUCED EMI

The choice of how aggressively EMI must be addressed for a design to pass emissions levels depends on the requirements of the design as well as cost and performance trade-offs.

The starting point for this example is a 2-layer PCB. EMI reductions are relative to the emissions and noise from this board. To conform to FCC Class B levels, the emissions at these two frequencies must be less than 46 dBµV/m, normalized to 3 m antenna distance. As expected, EMI testing confirmed that the largest emissions peaks occur at the tank frequency and rectifier frequency.

A 6-layer PCB that employs edge guarding and buried capacitive bypassing, which are EMI mitigation techniques described in detail in Application Note AN-0971, was manufactured. The stackup of the 6-layer test PCB is shown in Table 9. PCB layout Gerber files are available upon request.

Table 9. PCB Layers

Layer	Description
Top	Components and ground planes
Inner Layer 1	V_{CC} planes
Inner Layer 2	All tracks
Inner Layer 3	Blank
Inner Layer 4	Buried capacitive plane
Bottom	Ground planes

EMI testing was repeated on the optimized board. The resulting reduction in radiated emissions is shown in Table 10. This board meets FCC Class B standards with no external shielding by utilizing buried stitching capacitors and edge fencing.

Table 10. EMI Test Results

EMI Test Results	300 MHz	600 MHz
2-Layer PCB Emissions	48 dB	53 dB
6-Layer PCB Emissions	36 dB	32 dB
Achieved EMI Reduction	12 dB	21 dB

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions.

In the absence of logic transitions at the input for more than 1 µs, periodic sets of refresh pulses (indicative of the correct input state) are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state by the watchdog timer circuit. This situation should occur in the ADM3251E during power-up and power-down operations only.

The limitation on the ADM3251E magnetic field immunity is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The pulses at the transformer output have an amplitude of >1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\Sigma\pi r_n^2; \text{ n} = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil internally and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 22.

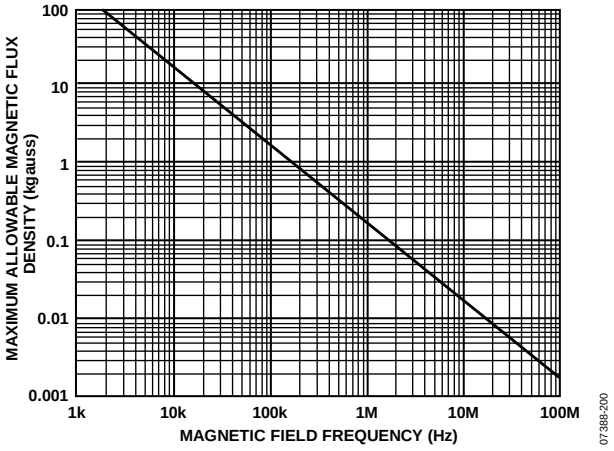


Figure 22. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the transformers. Figure 23 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 23, the ADM3251E is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For example, at a magnetic field frequency of 1 MHz, a 0.5 kA current placed 5 mm away from the ADM3251E is required to affect the operation of the component.

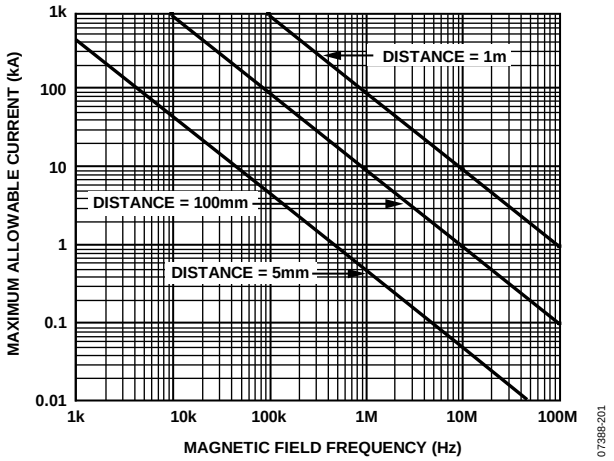


Figure 23. Maximum Allowable Current for Various Current-to-ADM3251E Spacings

In the presence of strong magnetic fields and high frequencies, any loops formed by PCB traces may induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

ISOLATED POWER SUPPLY CIRCUIT

To operate the ADM3251E with its internal dc-to-dc converter disabled, connect a voltage of between 3.0 V and 3.7 V to the V_{CC} pin and apply an isolated power of between 3.0 V and 5.5 V to the V_{ISO} pin, referenced to GND_{ISO}.

A transformer driver circuit with a center-tapped transformer and LDO can be used to generate the isolated supply, as shown in Figure 24. The center-tapped transformer provides electrical isolation of the 5 V power supply. The primary winding of the transformer is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP3330 linear voltage regulator provides a regulated power supply to the bus side circuitry (V_{ISO}) of the ADM3251E.

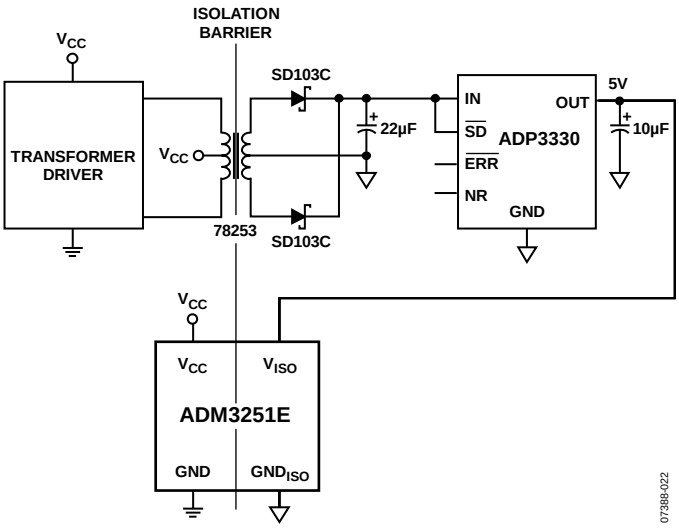
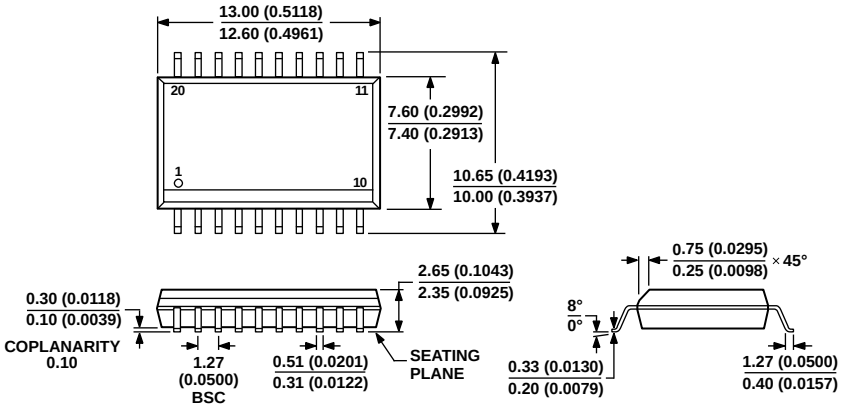


Figure 24. Isolated Power Supply Circuit

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

06-07-2006-A

Figure 25. 20-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-20)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM3251EARWZ	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
ADM3251EARWZ-REEL	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
EVAL-ADM3251EEB1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D07388-0-10/13(G)